

*A34S/A35S*

# *Schematics Document*

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Title

**Cover Page**

Size  
A4

Document Number

**A34S/A35S**

Rev  
**SB**

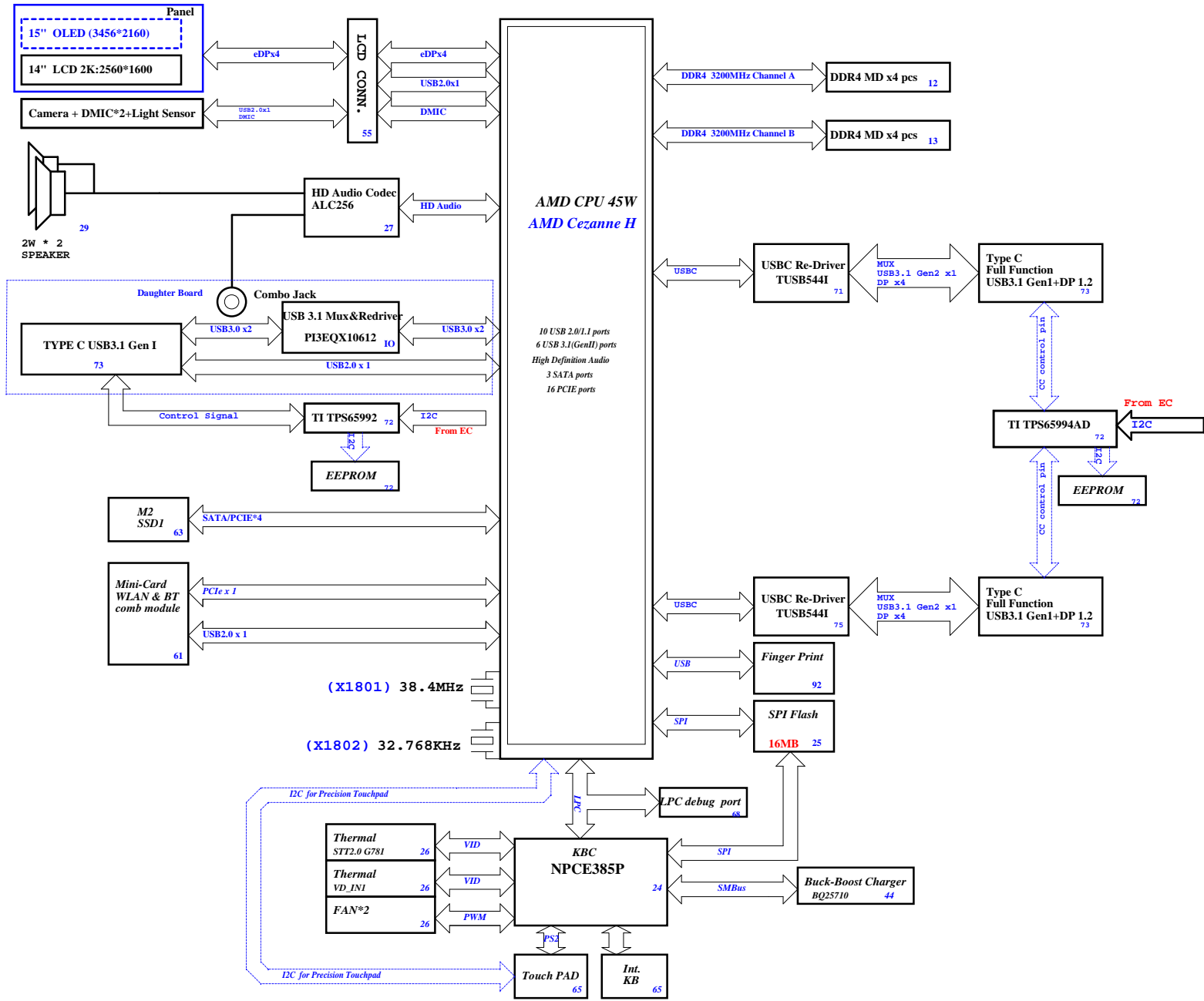
Date: Thursday, November 05, 2020

Sheet 1 of 106

*DY : None Installed*

Project Code:  
A34S 4PD0MV010001  
A35S 4PD0MT010001  
PCB No : 203031  
Revision : SB

# A34S/A35S Block Diagram



CHARGER BQ25710R		44
INPUTS	OUTPUTS	
PWR_AD_P_TOSYS	19V_DCBATOUT	BT
SYSTEM DC/DC SY8288CRAC		45
INPUTS	OUTPUTS	
19V_DCBATOUT	5V_AUX_S5	5V_S5
SYSTEM DC/DC SY8288BRAC		45
INPUTS	OUTPUTS	
19V_DCBATOUT	3D3V_AUX_S5	3D3V_S5
CPU DC/DC ISL62776HR/AOZ5038QI		46, 47
INPUTS	OUTPUTS	
19V_DCBATOUT	1V_CPU_CORE	
CPU DC/DC ISL62776HR/AOZ5049QI		46, 48
INPUTS	OUTPUTS	
19V_DCBATOUT	1D2V_CPU_SOC	
CPU DC/DC G5416QS1U		51
INPUTS	OUTPUTS	
19V_DCBATOUT	1D2V_S3	3D3V_S5
2D5V_S5		
CPU DC/DC SY8386RHC		52
INPUTS	OUTPUTS	
19V_DCBATOUT	0D75V_VDDP_S5	
SYSTEM DC/DC SY8386RHC		52
INPUTS	OUTPUTS	
19V_DCBATOUT	0D75V_VDDP_S0	
SYSTEM DC/DC G5335DQZ1U		53
INPUTS	OUTPUTS	
19V_DCBATOUT	1D8V_S5	
SYSTEM DC/DC RT9078		53
INPUTS	OUTPUTS	
19V_DCBATOUT	1D8V_AUX_S5	
SYSTEM Load switch G2898KD1U		40
INPUTS	OUTPUTS	
3D3V_S5	3D3V_S0	5V_S0
1D8V_S5	1D8V_S0	

**SSID = PCH**

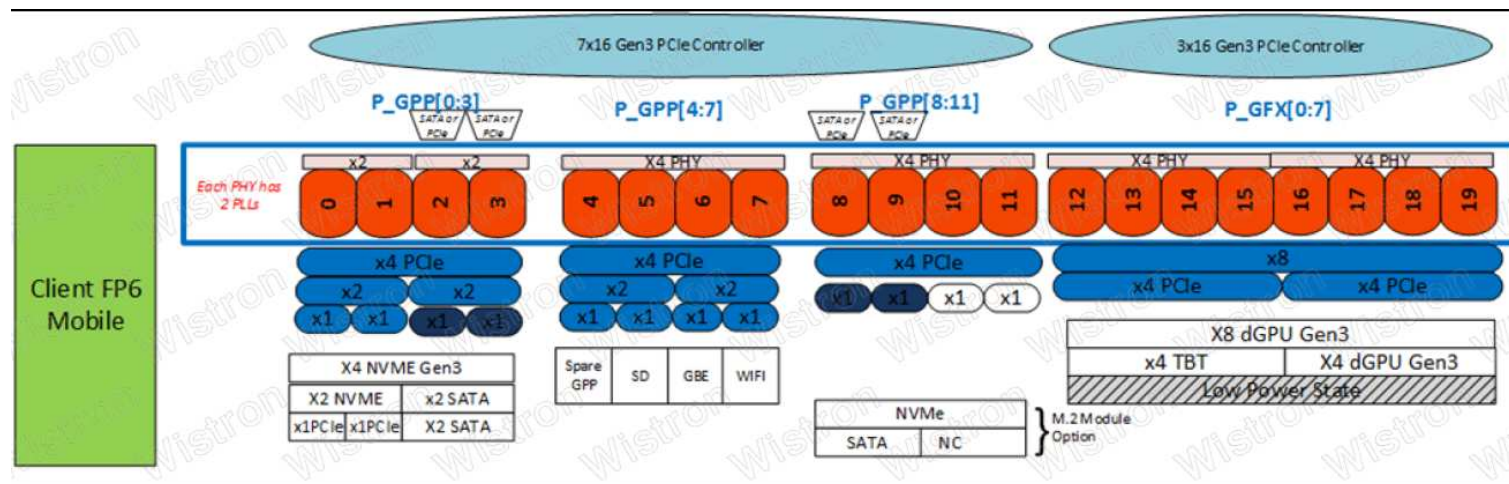
WLAN

**M.2 SSD (PCIe)**

WLAN

M.2 SSD (PCIe)

**WLAN**



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Title	<b>CPU (PCIe/SATA)</b>
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Size	Document Number
Custom	<b>A34S/A35S</b>


Rev	SB
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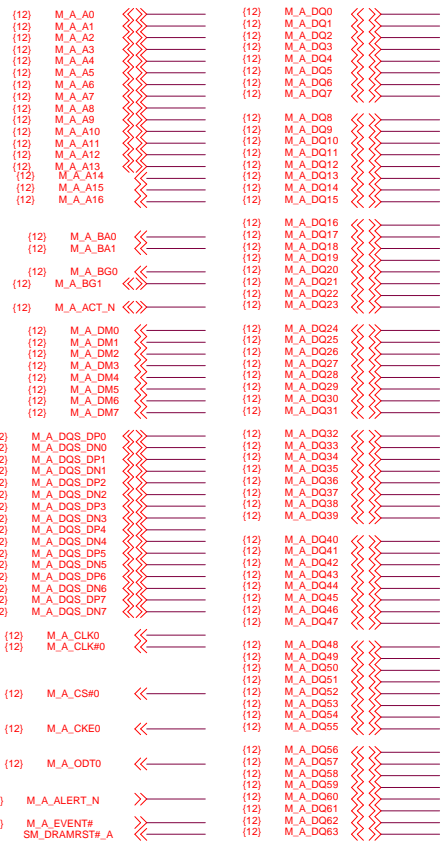
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Title <b>CPU (RSVD)</b>			
Size A4	Document Number <b>A34S/A35S</b>		Rev <b>SB</b>
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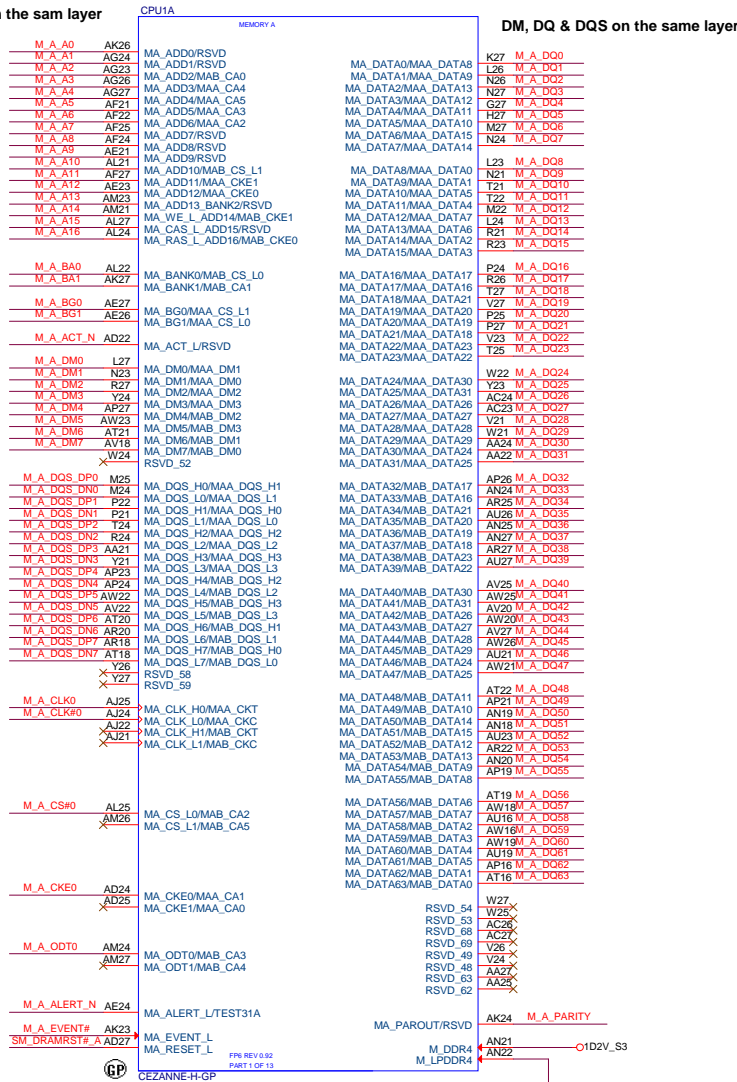


## DDR4 Channel A to Memory Down

DM, DQ & DQS on the same layer

ADD and CLK on the sam layer

ADD, CMD, CTL, 40Ω  
DATA, 50Ω  
Misc. 40-60Ω  
DDR CLK, 72Ω  
DQS, 80Ω



Layout Note:

DM, DQ & DQS on the same layer  
ADD and CLK on the sam layer

## STRAP PINS

	PIN NET <b>M_DDR4</b>	PIN NET <b>M_LDDR4</b>
PULL HIGH	Enable DDR4 memory controller 0ohm (± 5%) pull-up resistor or direct connect to VDDIO_MEM_S3 (DEFAULT)	Enable LPDDR4x memory controller 0ohm (± 5%) pull-up resistor or direct connect to VDDIO_MEM_S3 (DEFAULT)
PULL LOW	Disable DDR4 (need to have LPDDR4x enabled) 0ohm (± 5%) pull-down resistor or direct connect to VSS	Disable LPDDR4x (need to have DDR4 enabled) 0ohm (± 5%) pull-down resistor or direct connect to VSS (DEFAULT)

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CPU (DDR4 CHA)	
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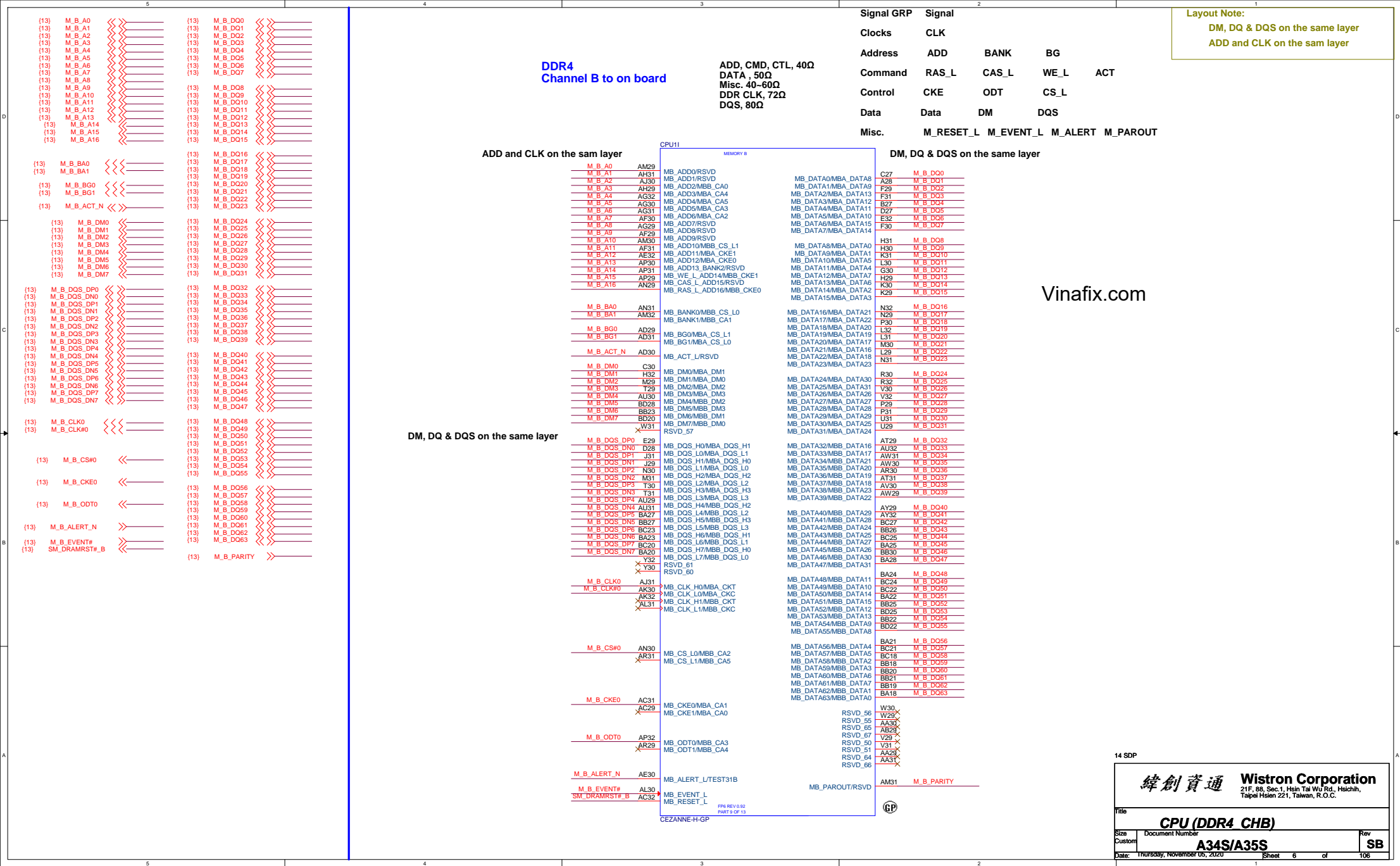
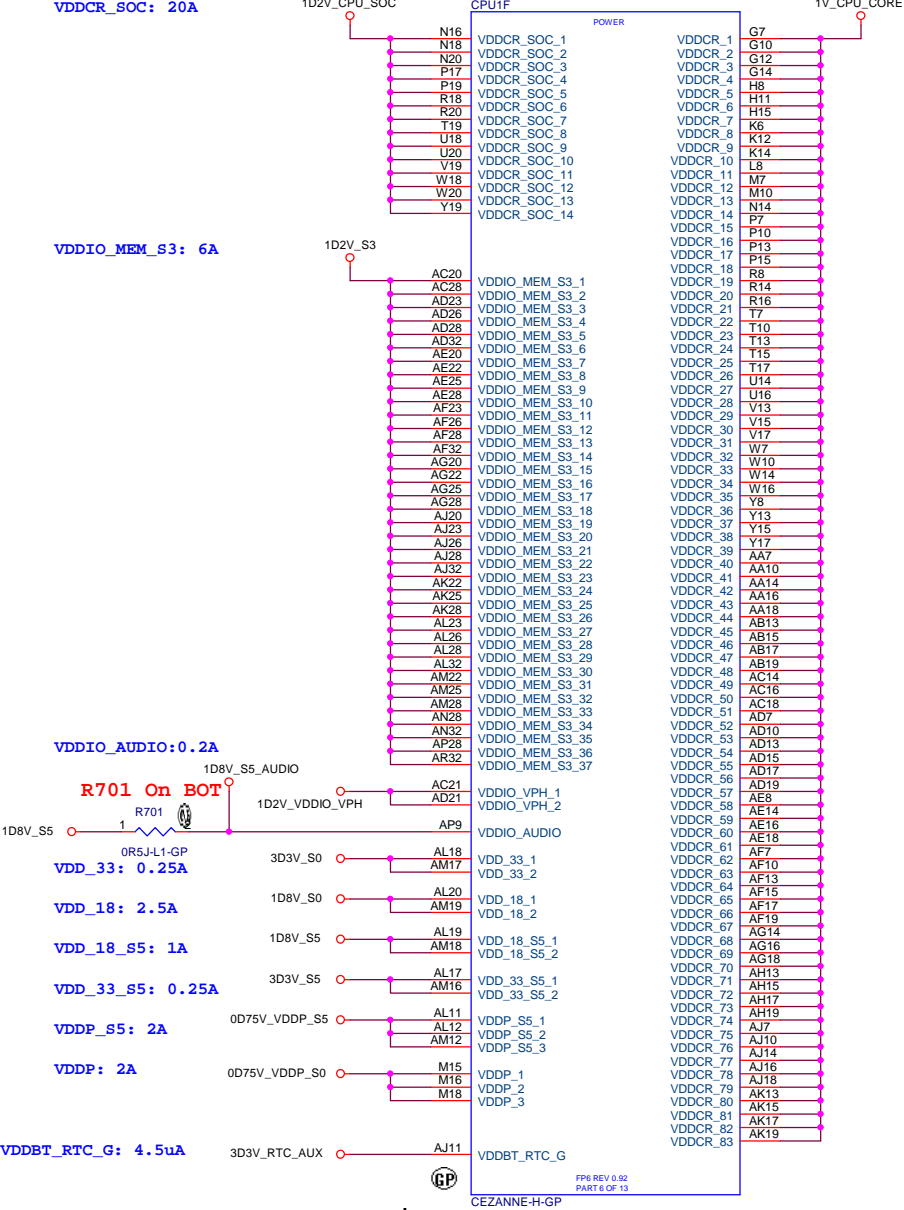


Table 8. FP6 Processor Voltage Supply Currents for AMD Family 19h Models 50h-5Fh Processors

Supply <sup>1</sup>	Nominal Voltage at Pkg Ball (V) <sup>2</sup>	Condition	SYSTEM_CONFIGURATION					
			1 10 W	2 15 W	3 25 W	4 35 W	5 45 W	6 54 W
VDDCR_VDD	Variable	TDC <sup>3</sup>	20	33	44	51		58
		EDC	70	90	95	105		110
	(0.6-1.55) <sup>5</sup>	Max Loadstep <sup>4</sup>	60	75	80	90		95
VDDCR_SOC	Variable	TDC <sup>3</sup>	10	13			15	
		EDC	13	17			20	
	(0.6-1.55) <sup>5</sup>	Max Loadstep <sup>4</sup>	10	13			15	
VDDIO_MEM_S3 <sup>6</sup>	1.10	TDC			6.00			
	1.20	TDC			6.00			
VDDIO_VPH <sup>7</sup>	1.20	TDC			1.00			
	1.80	TDC			1.00			
VDDP	0.75	TDC			2.00			
VDDP_S5	0.75	TDC			2.00			
VDD_18	1.80	TDC			2.50			
VDD_18_S5	1.80	TDC			1.00			
VDD_33	3.30	TDC			0.25			
VDD_33_S5	3.30	TDC			0.25			
VDDIO_AUDIO	1.20	TDC			0.20			
	1.50	TDC			0.20			
	1.80	TDC			0.20			
VDDBT_RTC_G	3.00	TDC			4.5 μA			



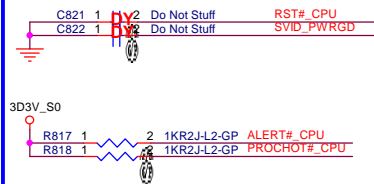
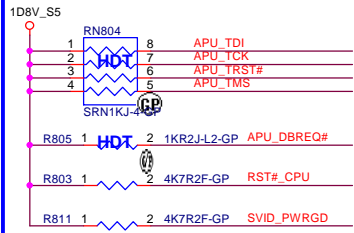
VDDIO_VPH	<p>VDDIO_VPH is a dedicated power supply for DisplayPort 0. When</p> <ul style="list-style-type: none"><li>DP0 is used for eDP, connect VDDIO_VPH to VDDIO_MEM_S3 source (1.1V LPDDR4x or 1.2V DDR4) to improve battery life</li><li>DP0 is used for DP or HDMI, connect VDDIO_VPH to VDD_18 source (1.8V)</li></ul>
-----------	--



# SSID = PCH

DisplayPort	Device
0	eDP
1	HDMIout

HDT PIN Pull High Resistor  
ASM if HDT CONN is needs of use



SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

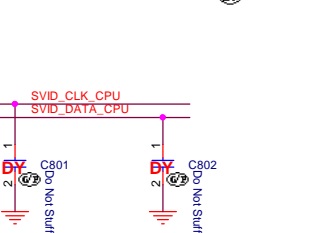
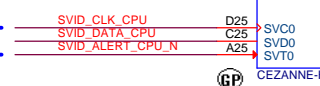
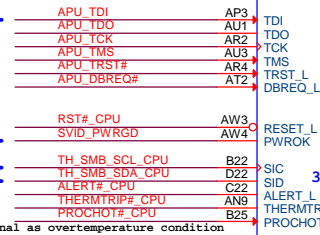
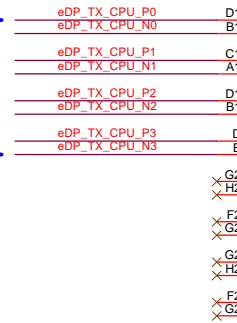


eDP

HDT

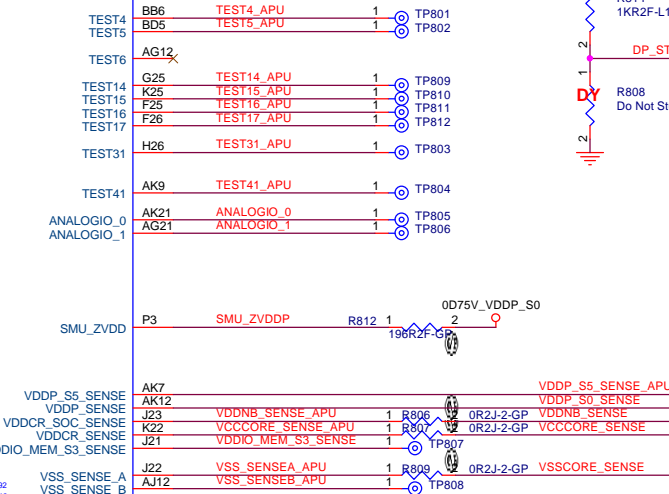
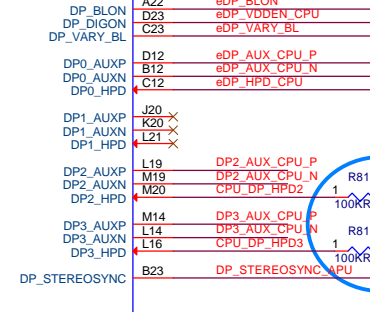
SMB  
to KBC , TH

SVID



CPU1C

DISPLAY/SVID/TAG/TEST



FP6 REV 0.02  
PART 3 OF 13

CEZANNE-H-GP

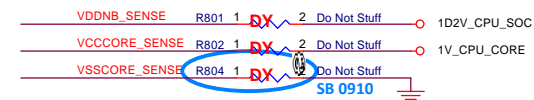
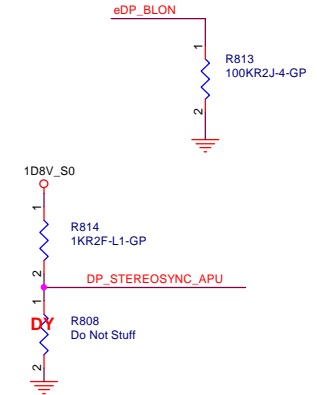
eDP

SB 0901

Table 6. LCD Power Section Pin Description

Signal Name	Type	Description	Pin
DP_BLOK	0A0104	Display Panel Backlight Enable	1 1
DP_DIGON	0A0104	Display Panel Power Enable	1 1
DP_STEREO SYNC	0A0104	Signal used to drive stereo display glasses for stereoscopic 3D viewing at 120Hz refresh	1 1
DP_VARY_BL	0A0104	Display Backlight Brightness Control	1 1

PINOUT	Description
DP_BLOK	BL_ENABLE
DP_DIGON	LCD_VCC_ENABLE
DP_VARY_BL	BL_PWM



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Title	CPU (DP/SVID/HDT/TEST)		
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VSS

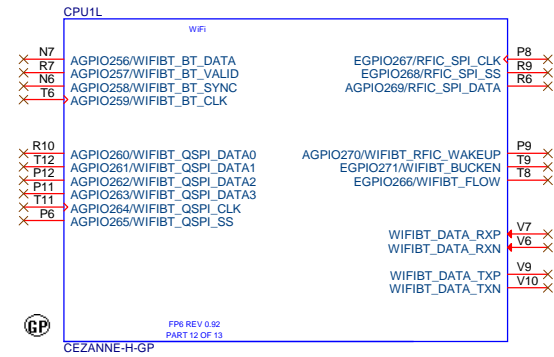
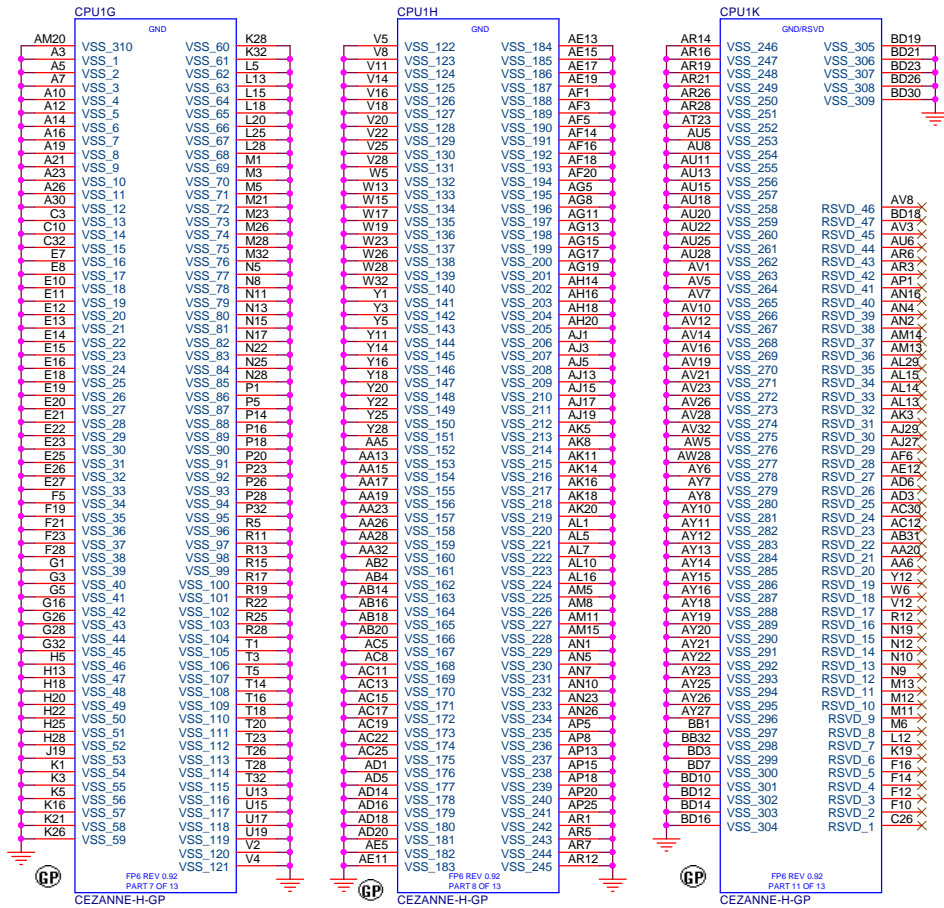
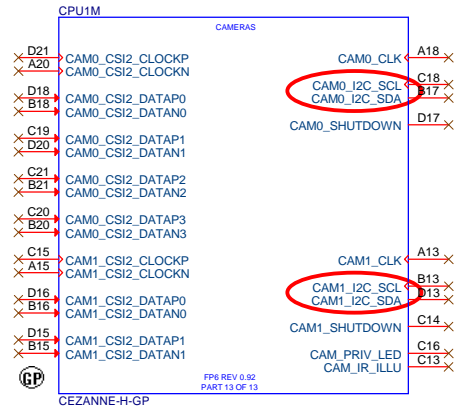


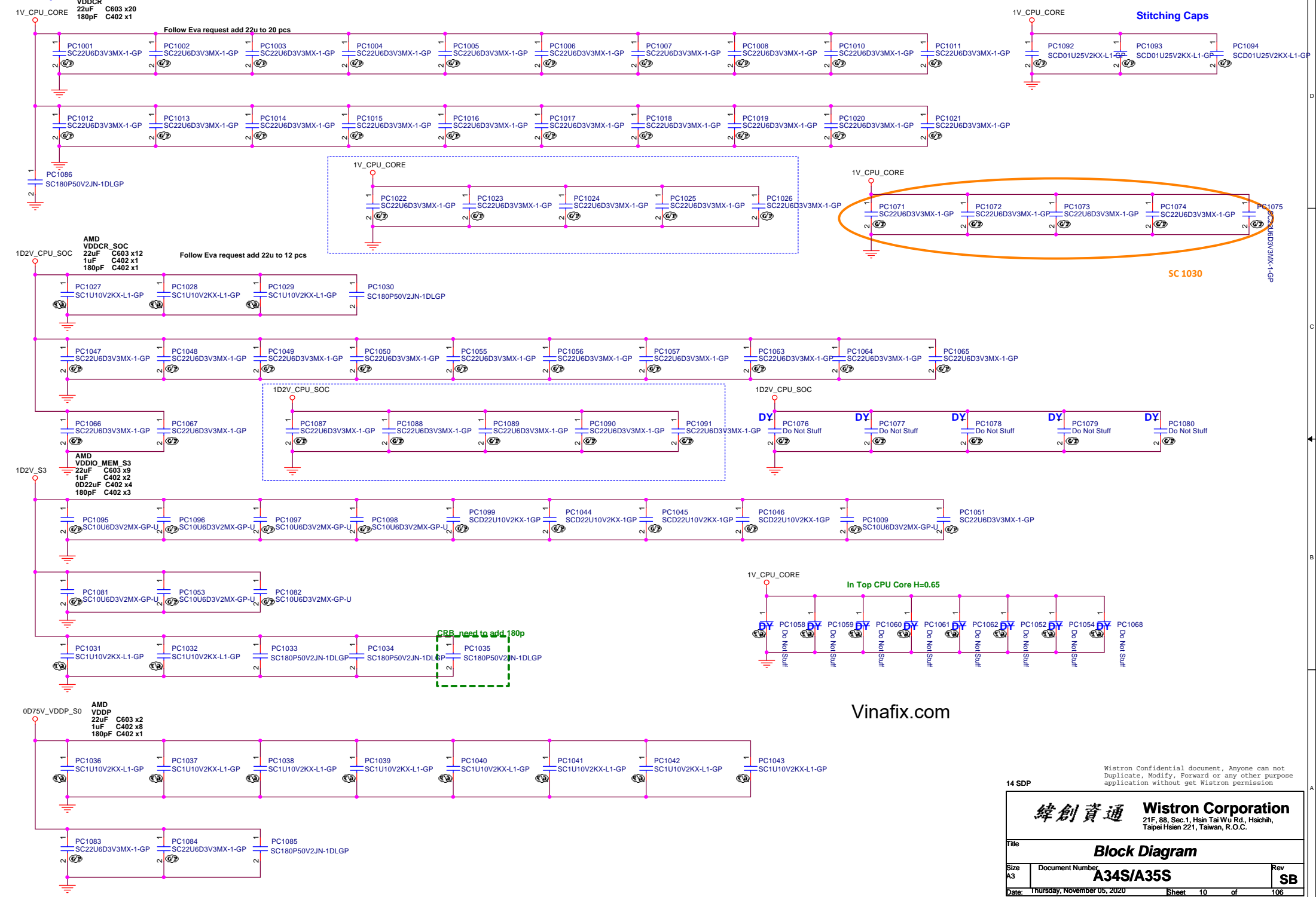
Table 22. WiFi Pin Description - Not Supported  
Document Number: 56177 Ver0.5



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APU Caps

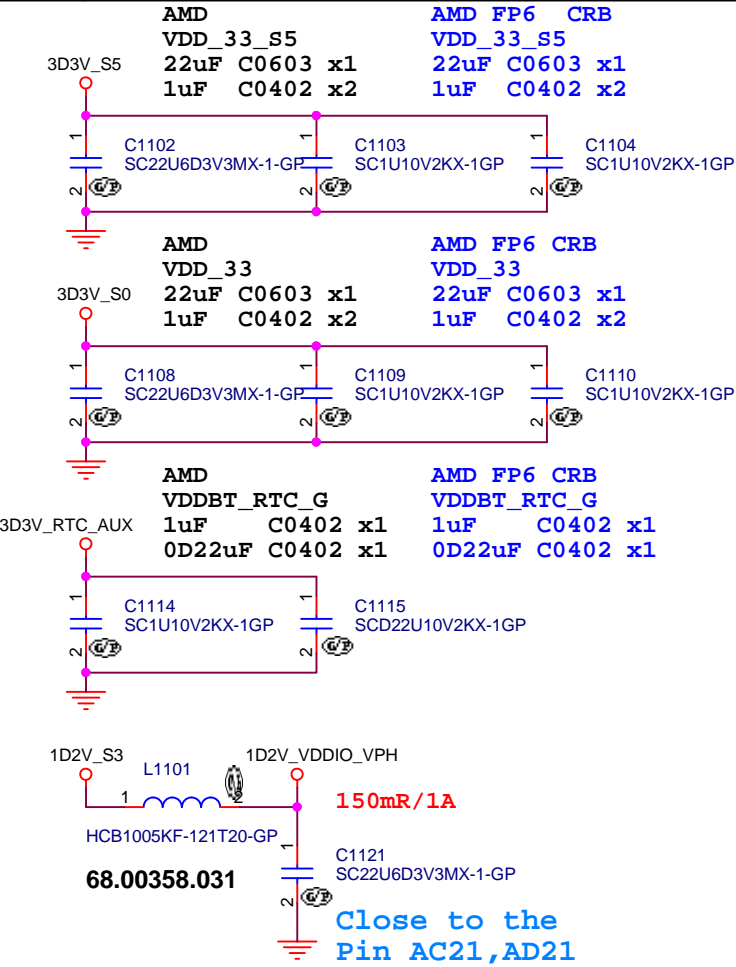
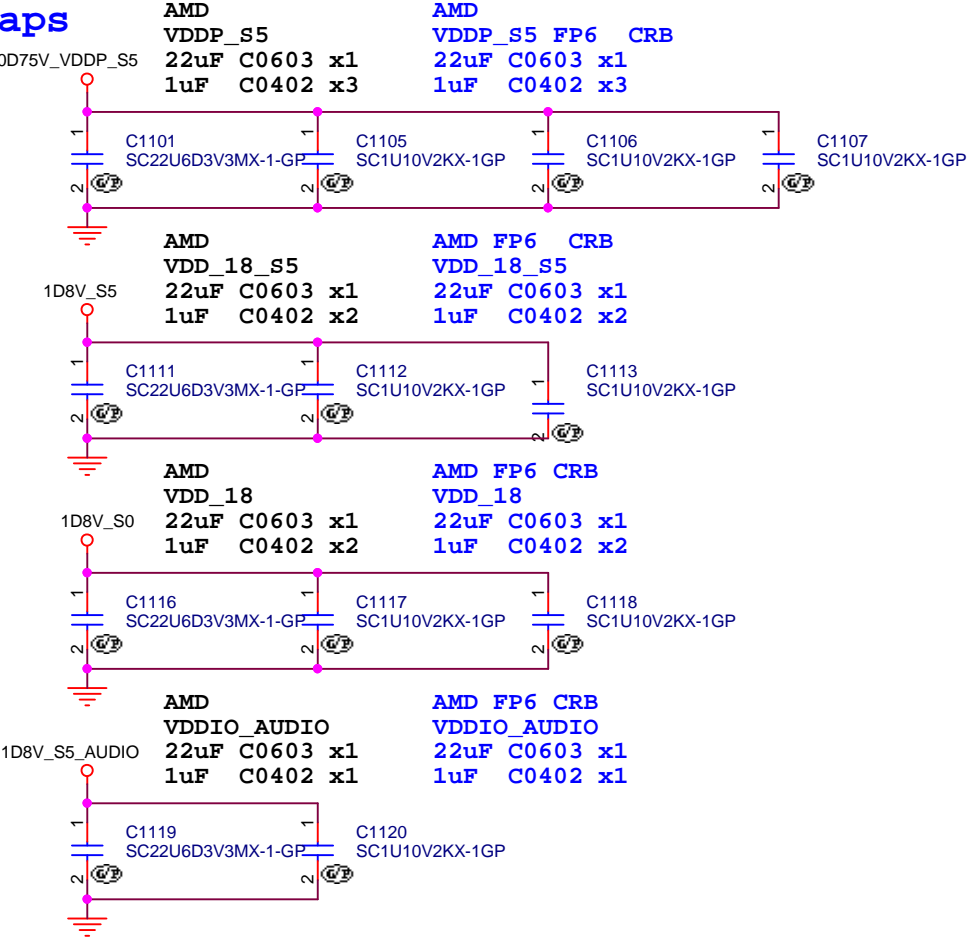


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Title Block Diagram		
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APU Caps



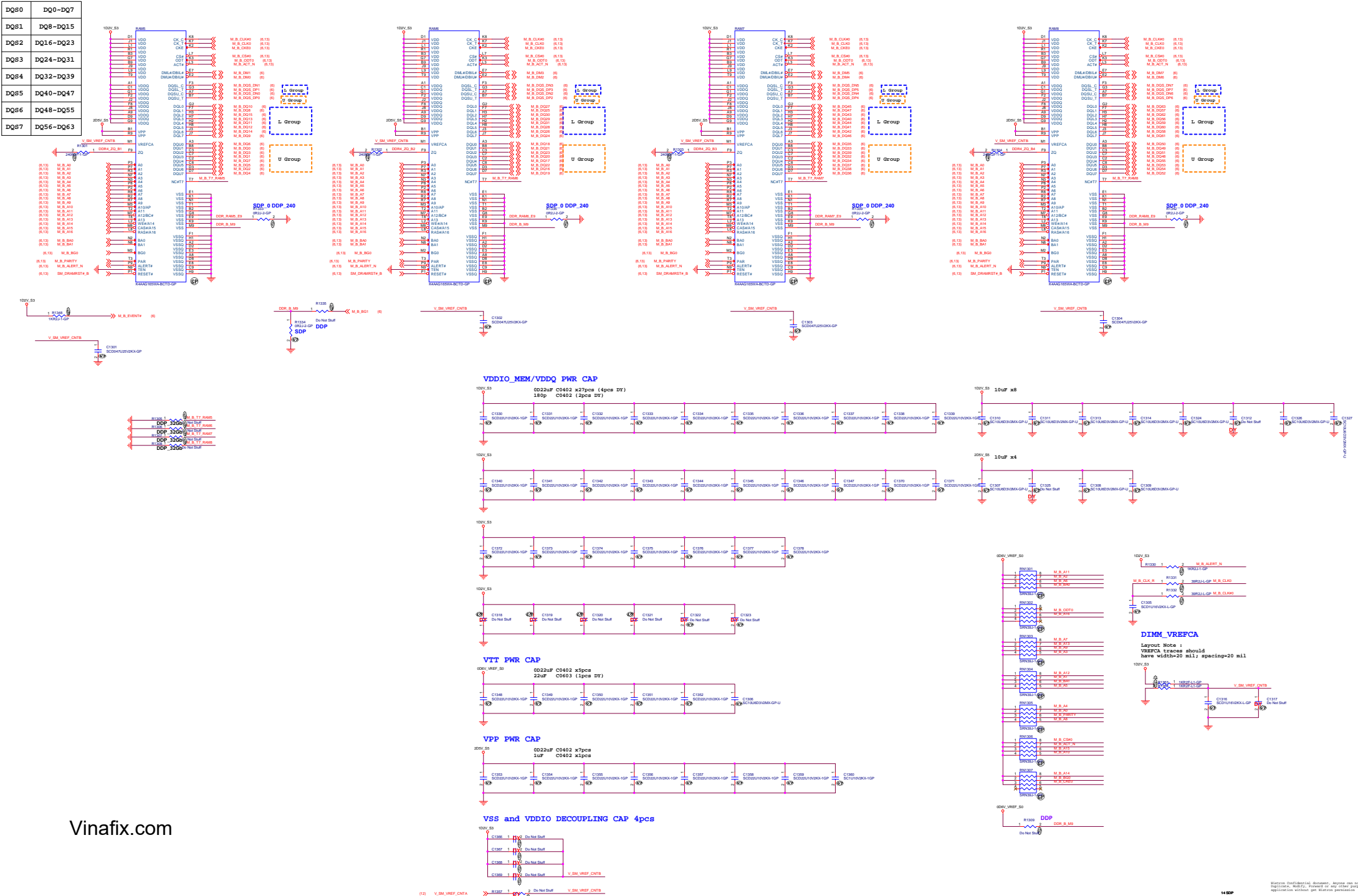
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<b>CPU (POWER CAP2)</b>			
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DQ80	DQ0~DQ7
DQ81	DQ8~DQ15
DQ82	DQ16~DQ23
DQ83	DQ24~DQ31
DQ84	DQ32~DQ39
DQ85	DQ40~DQ47
DQ86	DQ48~DQ55
DQ87	DQ56~DQ63



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Title <b>DDR (RSVD)</b>			
Size A4	Document Number <b>A34S/A35S</b>		Rev <b>SB</b>
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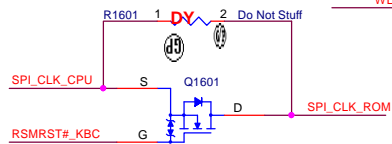
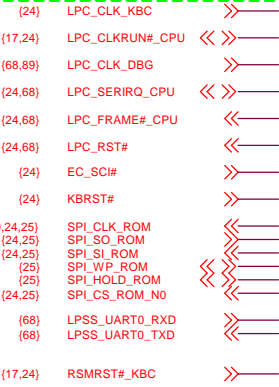
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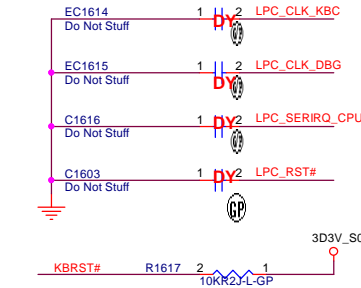
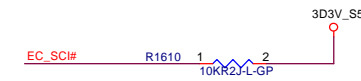
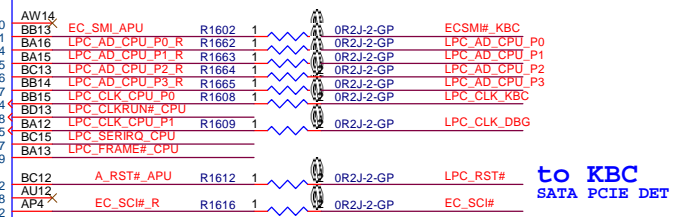
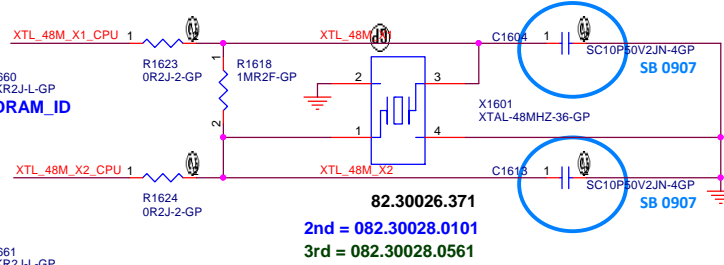
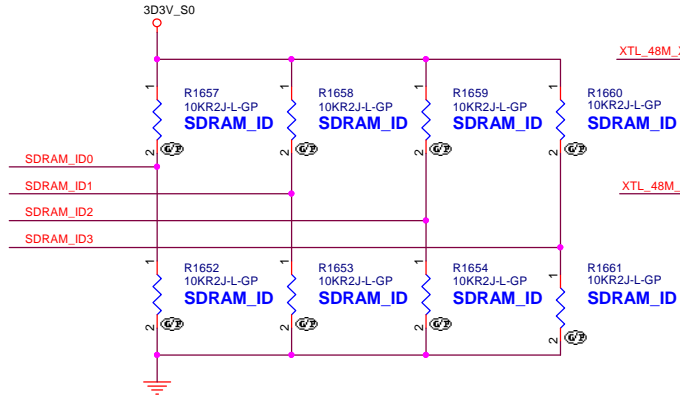
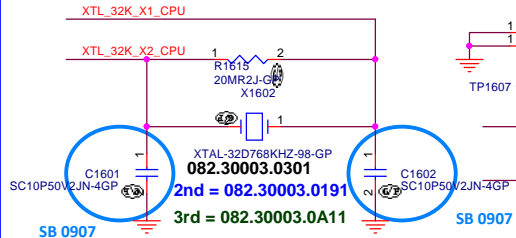
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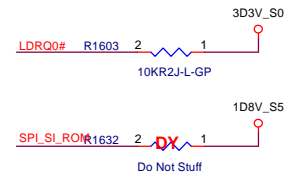
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{61}	WLAN_CLKREQ_CPU_N	>>>
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{61}	WLAN_CLK_CPU_P	<<<
{61}	WLAN_CLK_CPU_N	<<<
{17}	ECSMI#_KBC	>>>



LPCCCLK1/EGPIO75  
CLK\_REQ5\_L  
If unused,  
enable internal pull up or pull down by software.



								AN15	AN13	AN11	AR15
								EGPIO121	EGPIO120	EGPIO132	AGPIO116
								SDRAM_ID4	SDRAM_ID2	SDRAM_ID1	SDRAM_ID0
Memory	DDR4 16G	MM20000013725	Memory 16Gb 1z SDP DDR4 3200M Micron	MT40A1G16KD-062E:E	Micron	SDP	0	0	0	0	
		MM20000077820	Memory 16Gb A-Die DDR4 SDRAM 3200M Sam	K4AAG165WA-BCWE	Samsung	SDP	0	0	0	1	
	DDR4 8G	MM20000013625	Memory 8Gb 1y DDR4 DRAM 3200M Micron	MT40A512M16TB-062E:J	Micron	SDP	0	0	1	0	
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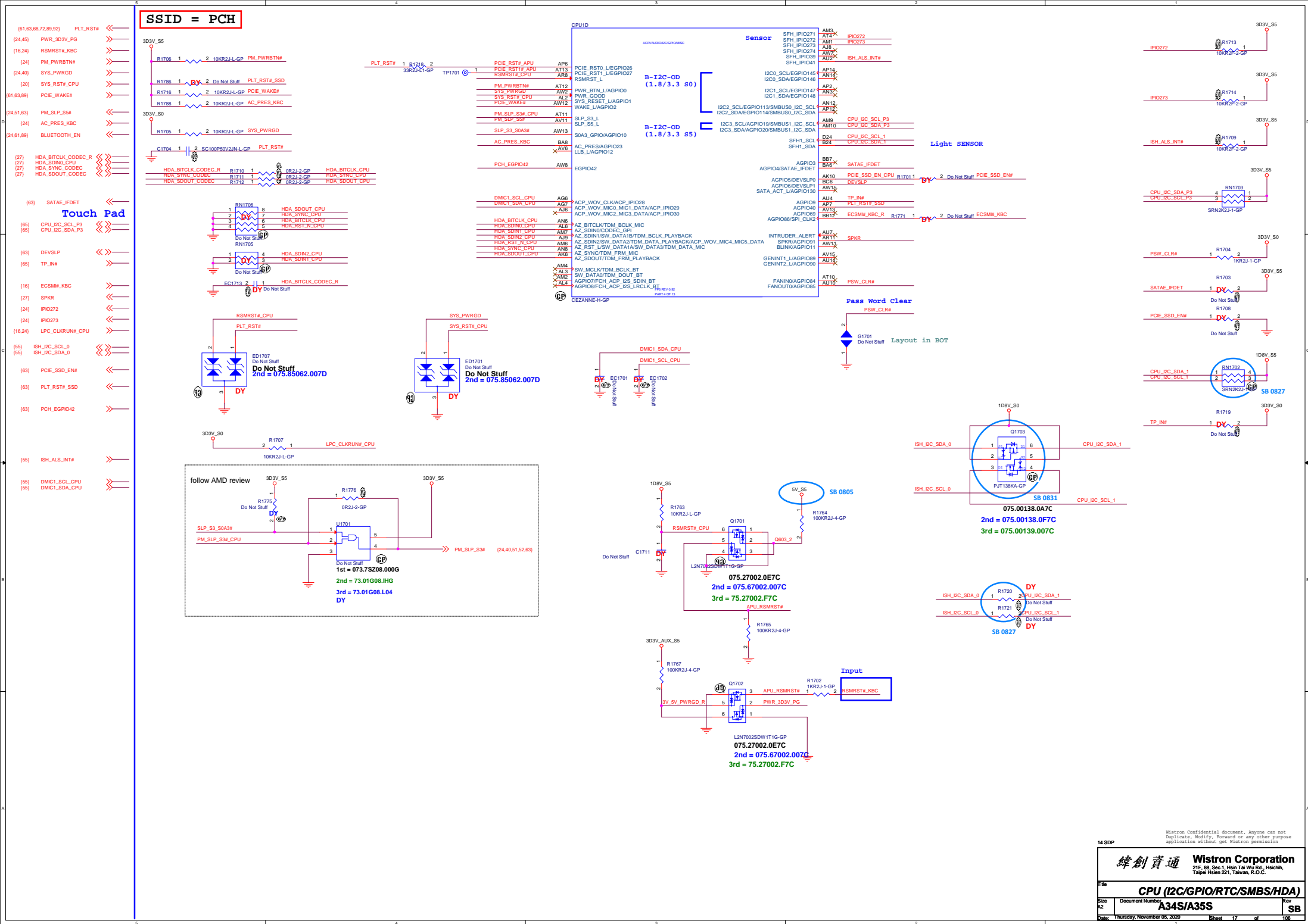
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Title	<b>CPU (CLK/LPC/SPI/UART)</b>
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Size A3	Document Number <b>A34S/A35S</b>	Rev SE
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# Main Func = USB

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{73} USB1\_USB20\_N

## U2 Type-C (IO)

{66} USB3\_USB20\_P  
{66} USB3\_USB20\_N

## U2 Type-C (MB)

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{73} USB2\_USB20\_N

## CCD

{55} CCD\_USB20\_N  
{55} CCD\_USB20\_P

## BT

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{61} BT\_USB20\_N

## FP

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{92} FP\_USB20\_P

## MB TypeC

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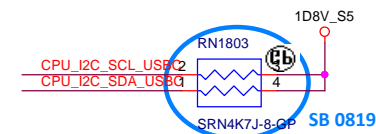
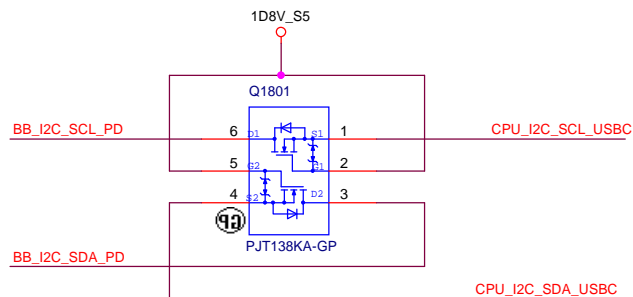
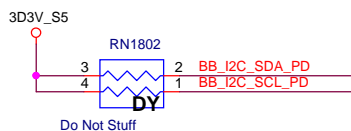
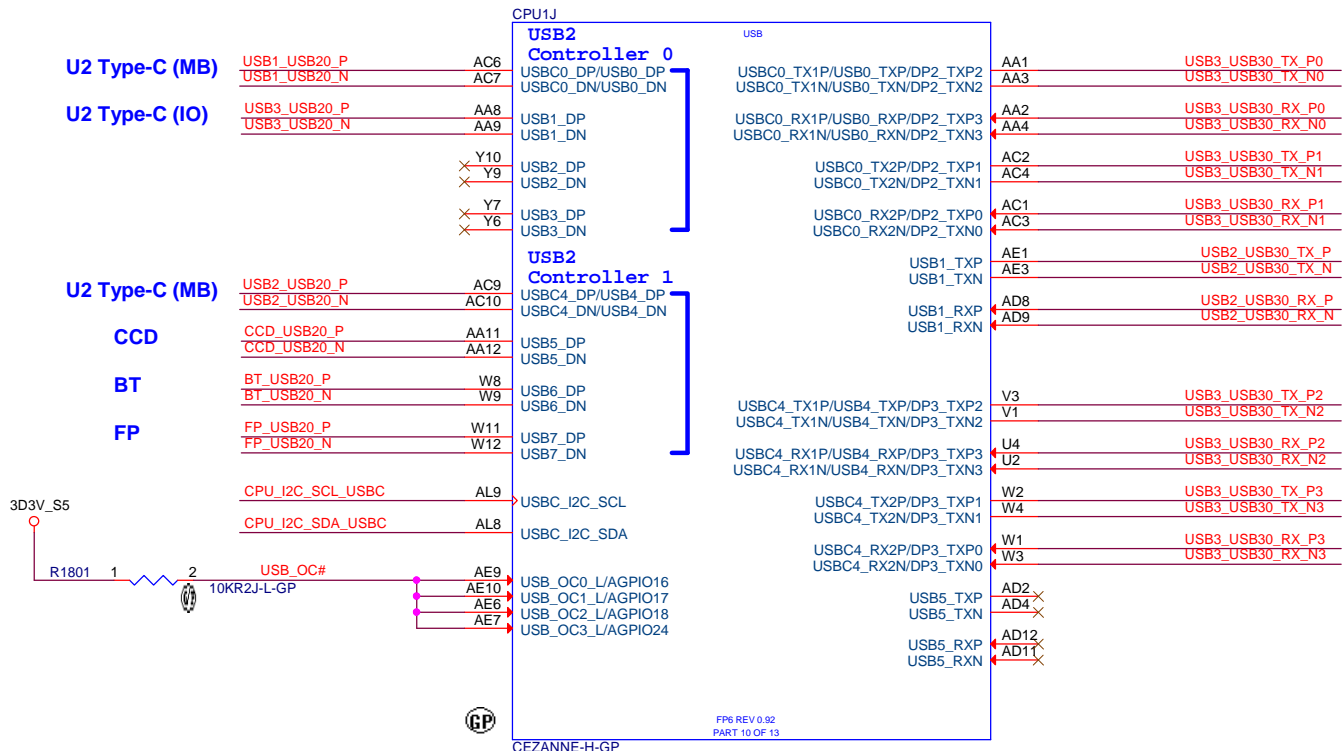
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{75} USB3\_USB30\_RX\_N3

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{71,72,75} BB\_I2C\_SDA\_PD



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CPU (USB)			
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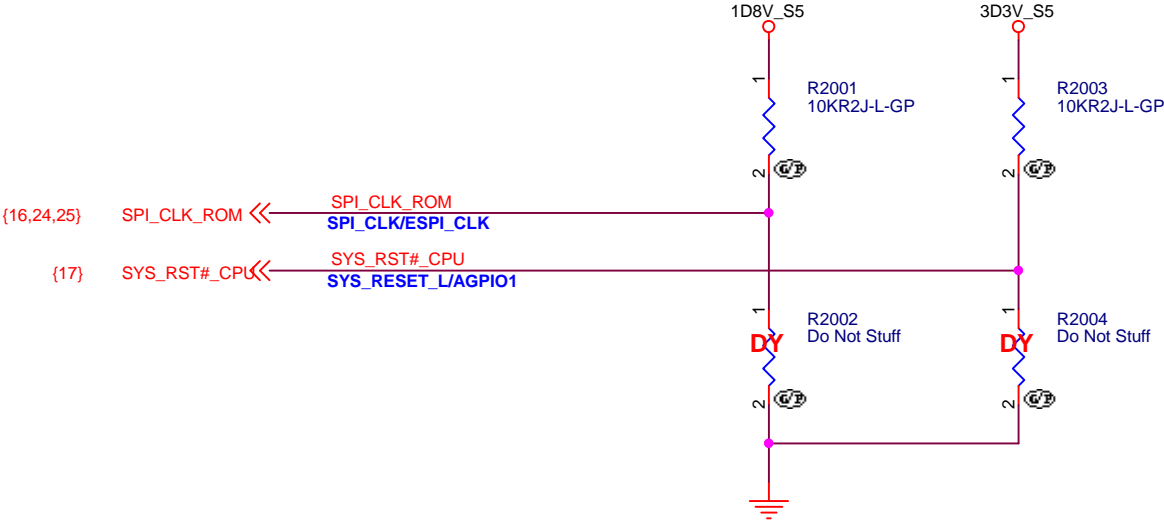
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STRAP PINS



	FUNCTION	DEFINTION
SPI_CLK		1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS (DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RST#		1:NORMAL RESET MODE (DEFAULT) 0:SHORT RESET MODE

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Title

CPU (Strap)

Size  
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Title <b>CPU (RSVD)</b>			
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Date <div>Thursday, November 05, 2020</div>		Sheet <div>23</div> of <div>106</div>

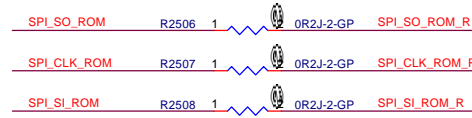
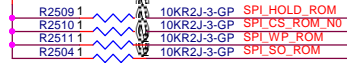


## Main Func = SPI Flash

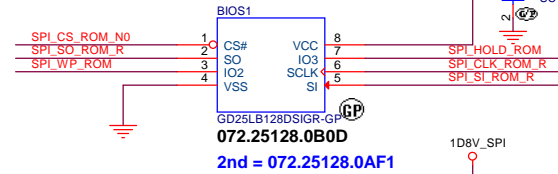
16MByte

SPI ROM Equal length need to less than 500mil

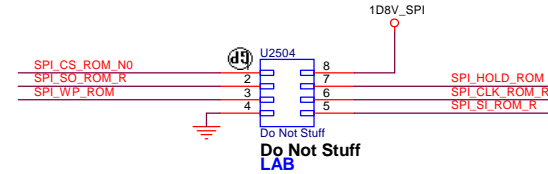
1D8V\_SPI



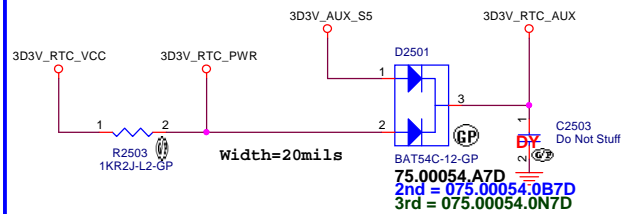
R2502 On BOT



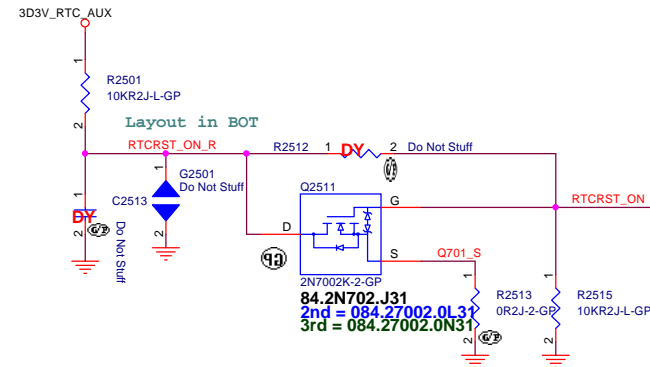
GD WINBOND GD25LB128DSIGR  
W25Q128JWSIQT



## Main Func = RTC



RTC BATTERY  
1st= TBD



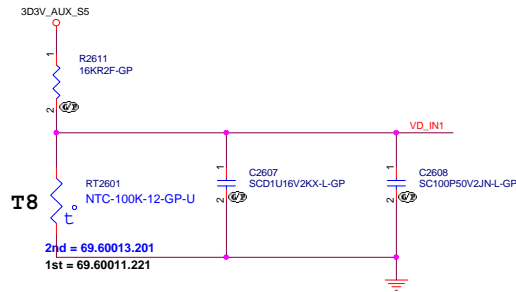
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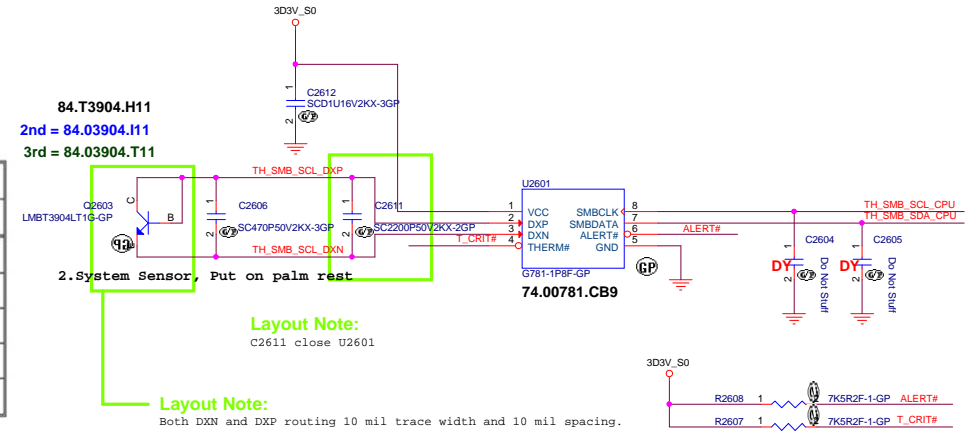
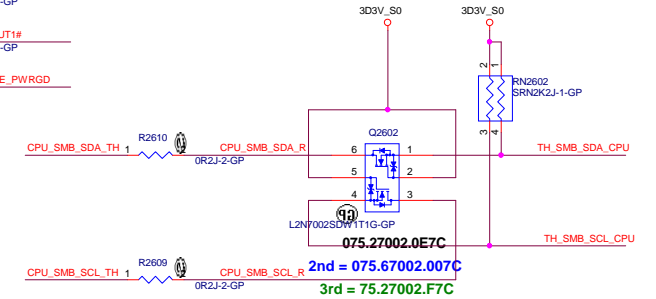
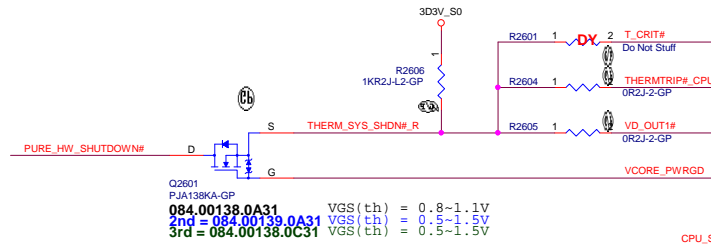
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Title		Flash/RTC	
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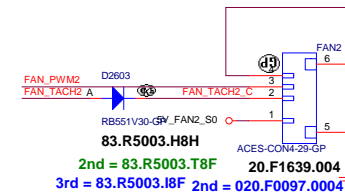
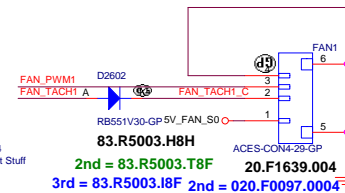
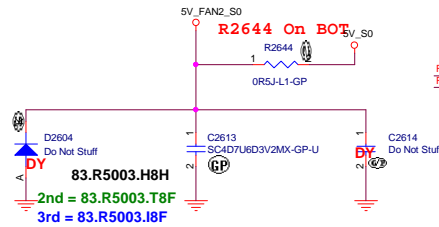
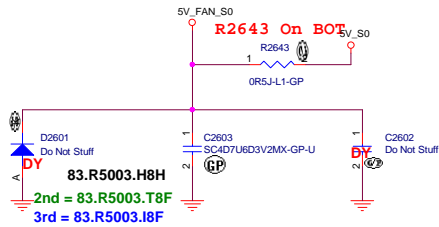
# SSID = Thermal



TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



\*Layout\* 15 mil



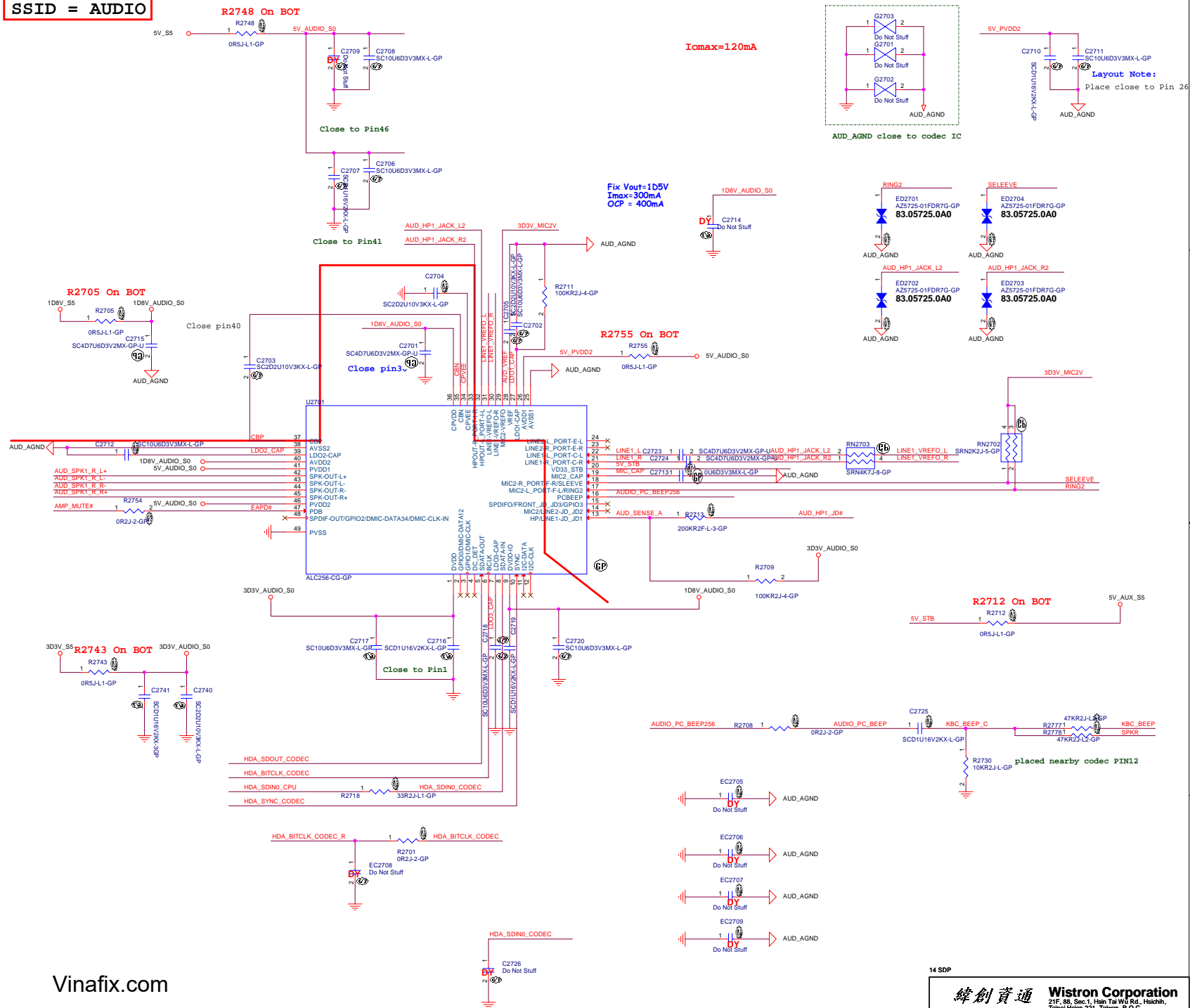
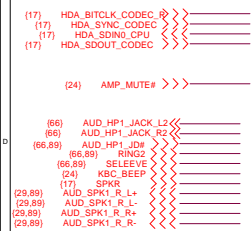
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SSID = AUDIO



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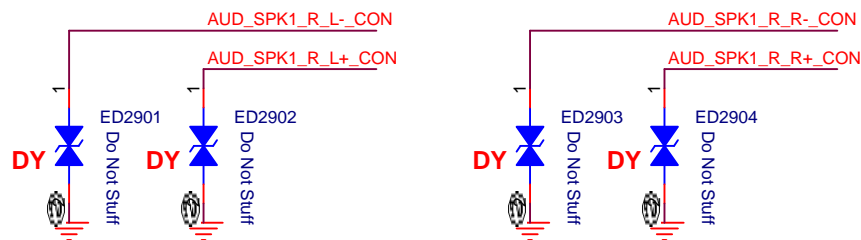
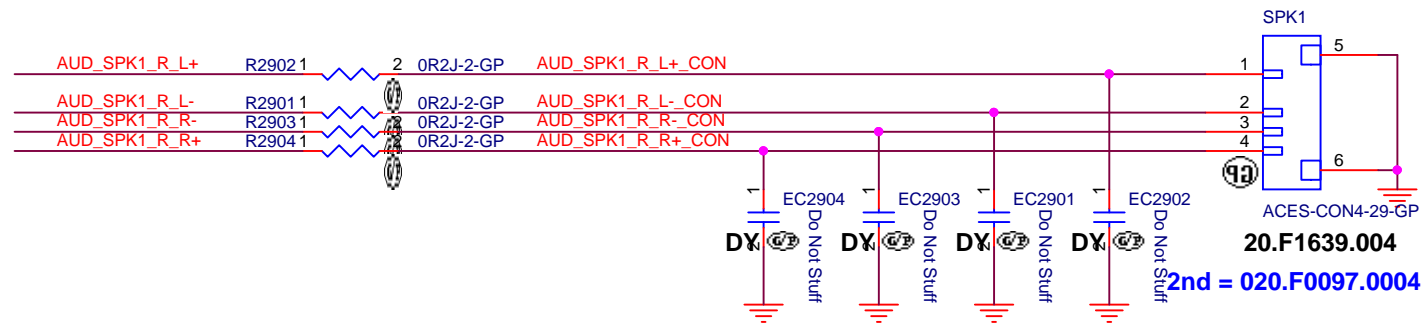
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# SSID = AUDIO Speaker

(27.89) AUD\_SPK1\_R\_L-  
(27.89) AUD\_SPK1\_R\_L+  
(27.89) AUD\_SPK1\_R\_R-  
(27.89) AUD\_SPK1\_R\_R+  
(27.89) AUD\_SPK1\_R\_R+  
(27.89) AUD\_SPK1\_R\_R+



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Title

**Audio (Speaker/HPMIC)**

Size  
A4

Document Number

**A34S/A35S**

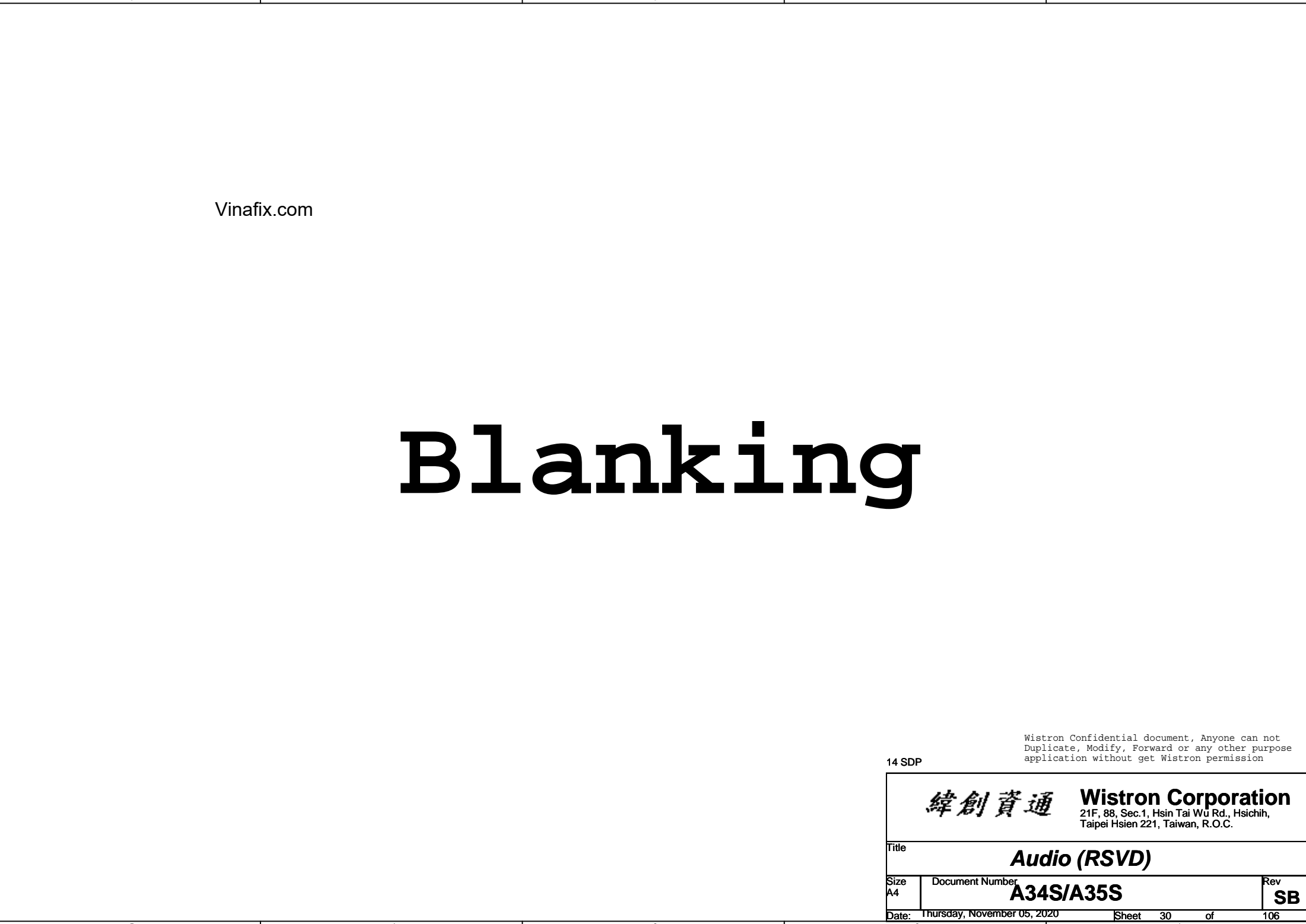
Rev

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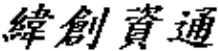


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Title

**LAN (RSVD)**

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Document Number

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Rev

**SB**

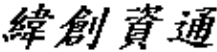
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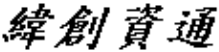
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Title

**USB (RSVD)**

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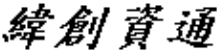
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Title <b>USB (RSVD)</b>			
Size A4	Document Number <b>A34S/A35S</b>		Rev <b>SB</b>
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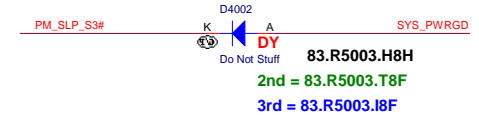
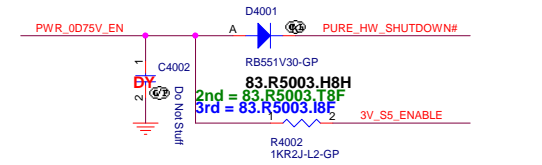
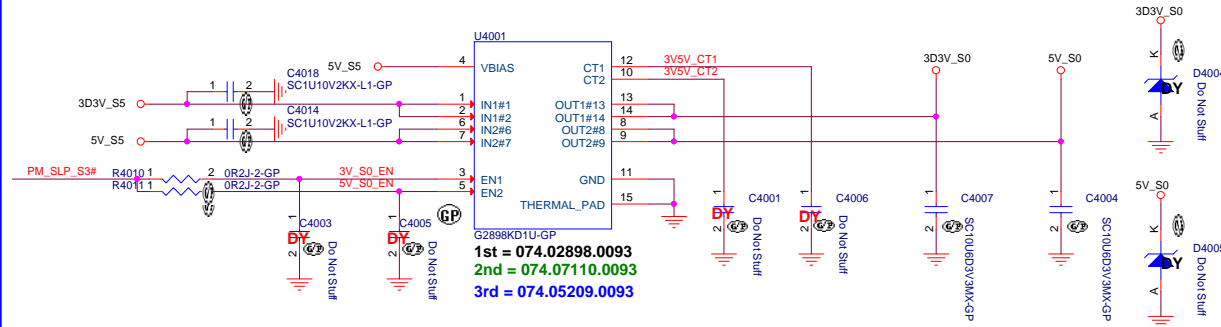
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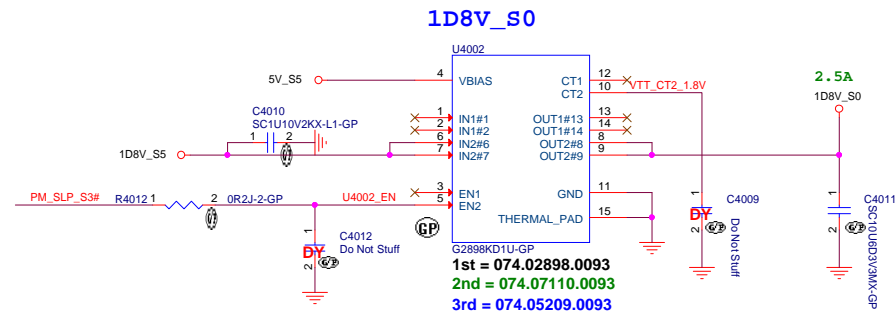
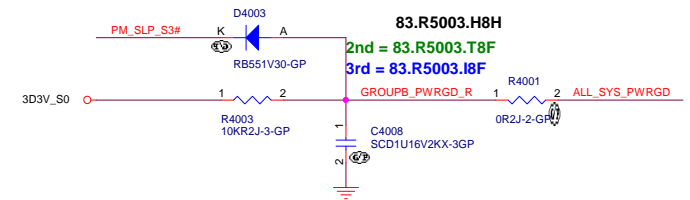
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Title <b>Sequence (RSVD)</b>			
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## Power Sequence

3D3V\_S5, 5V\_S5



Delay for S0\_PWRGD to VCORE\_EN



## A6S ET CPU 漏電 issue

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### Sequence (Power Plane EN)

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5

4

3

2

1

D

D

C

C

B

B

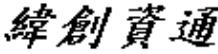
A

A

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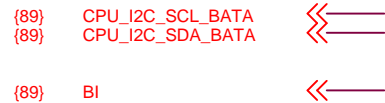
5

4

3

2

1



緯創資通

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2017	Journal of Chemical Education	94	2	321-328
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2016	Journal of Chemical Education	93	1	123-130
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2015	Journal of Chemical Education	92	4	567-574
5. The Effect of Catalyst on the Rate of Reaction	David Green	2014	Journal of Chemical Education	91	5	678-685

### INT 10 (DC IN/BAT CON)

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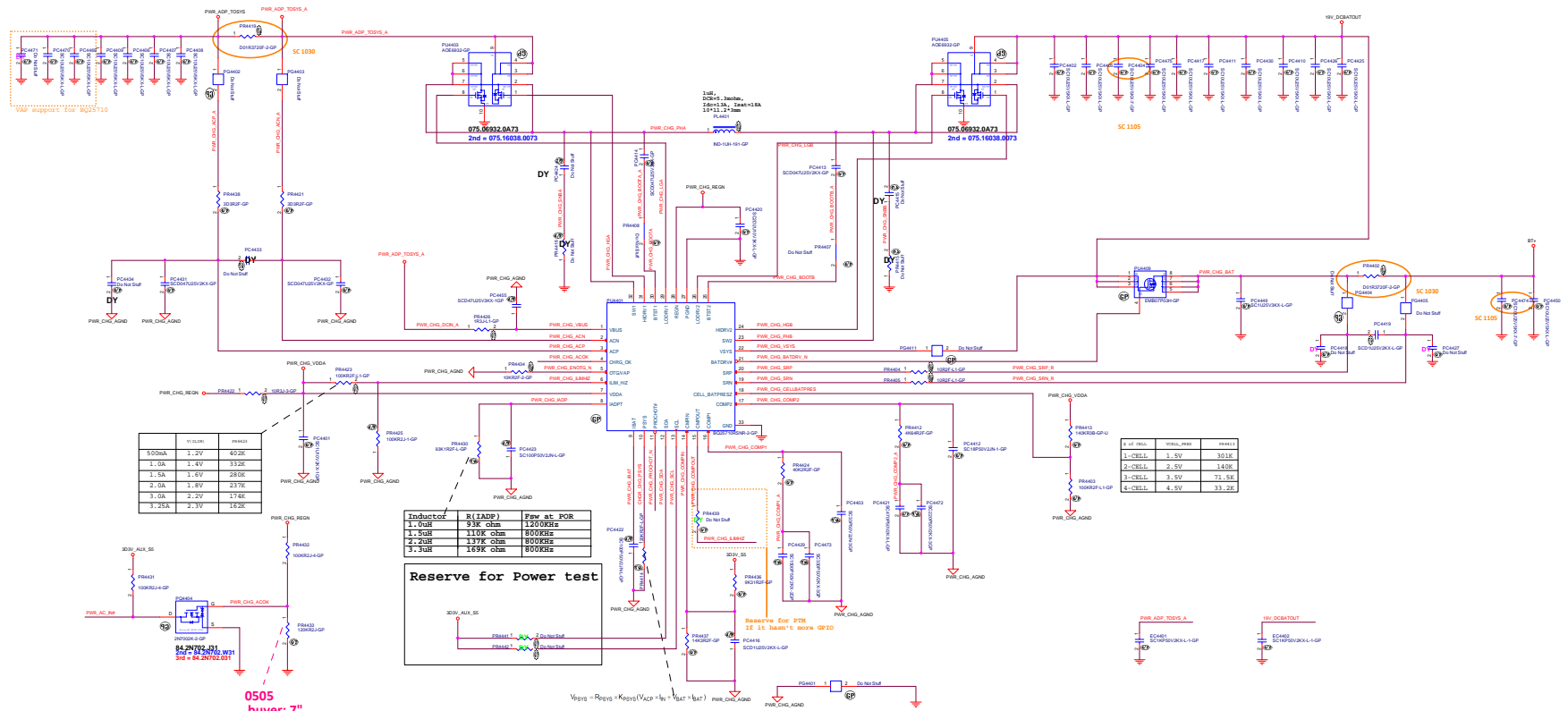


Figure 1: Schematic representation of the chemical synthesis of the poly(arylene ether)s. The scheme shows the reaction of 1,4-bis(hydroxy)benzene (HOB) with various diisocyanates (OCN-Ar-NCO) in the presence of a catalyst (PbAc<sub>2</sub>) and a base (Pb(OAc)<sub>4</sub>) to form poly(arylene ether)s. The resulting polymers are labeled with their respective diisocyanate units: P(Ar), P(Ar-1), P(Ar-2), P(Ar-3), P(Ar-4), P(Ar-5), P(Ar-6), P(Ar-7), P(Ar-8), P(Ar-9), P(Ar-10), P(Ar-11), P(Ar-12), P(Ar-13), P(Ar-14), P(Ar-15), P(Ar-16), P(Ar-17), P(Ar-18), P(Ar-19), P(Ar-20), P(Ar-21), P(Ar-22), P(Ar-23), P(Ar-24), P(Ar-25), P(Ar-26), P(Ar-27), P(Ar-28), P(Ar-29), P(Ar-30), P(Ar-31), P(Ar-32), P(Ar-33), P(Ar-34), P(Ar-35), P(Ar-36), P(Ar-37), P(Ar-38), P(Ar-39), P(Ar-40), P(Ar-41), P(Ar-42), P(Ar-43), P(Ar-44), P(Ar-45), P(Ar-46), P(Ar-47), P(Ar-48), P(Ar-49), P(Ar-50), P(Ar-51), P(Ar-52), P(Ar-53), P(Ar-54), P(Ar-55), P(Ar-56), P(Ar-57), P(Ar-58), P(Ar-59), P(Ar-60), P(Ar-61), P(Ar-62), P(Ar-63), P(Ar-64), P(Ar-65), P(Ar-66), P(Ar-67), P(Ar-68), P(Ar-69), P(Ar-70), P(Ar-71), P(Ar-72), P(Ar-73), P(Ar-74), P(Ar-75), P(Ar-76), P(Ar-77), P(Ar-78), P(Ar-79), P(Ar-80), P(Ar-81), P(Ar-82), P(Ar-83), P(Ar-84), P(Ar-85), P(Ar-86), P(Ar-87), P(Ar-88), P(Ar-89), P(Ar-90), P(Ar-91), P(Ar-92), P(Ar-93), P(Ar-94), P(Ar-95), P(Ar-96), P(Ar-97), P(Ar-98), P(Ar-99), P(Ar-100).

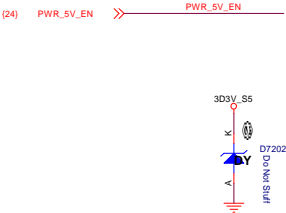
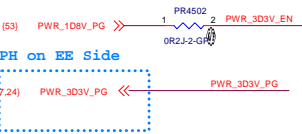
Reserve for Power test
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0505  
buyer: 7"

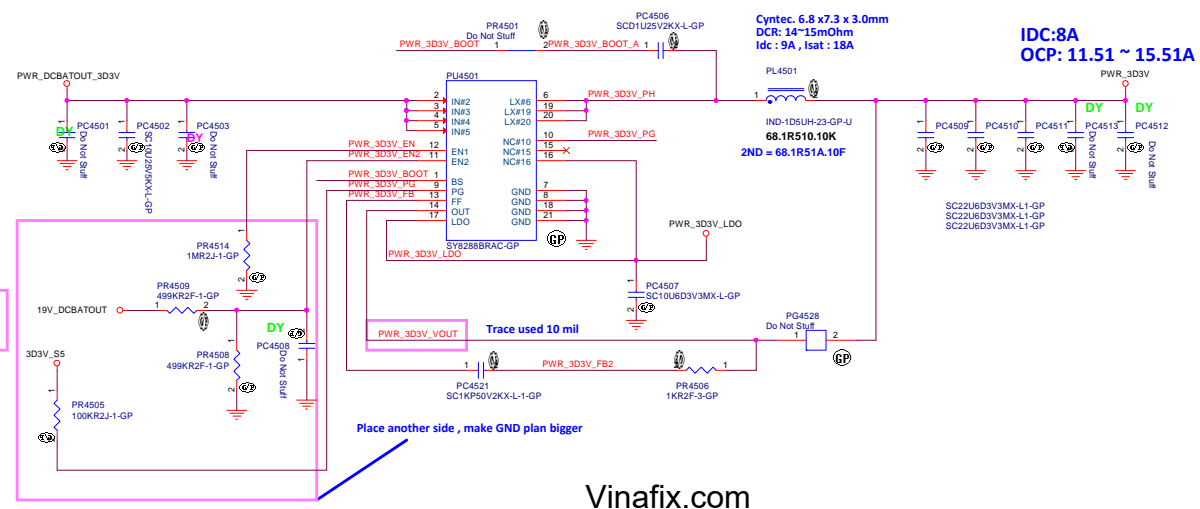
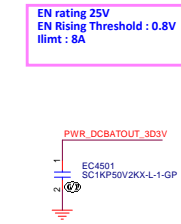
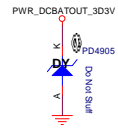
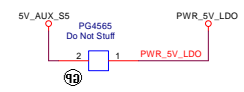
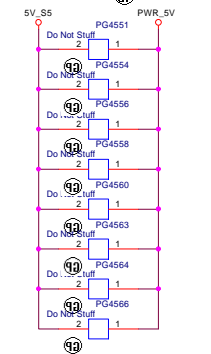
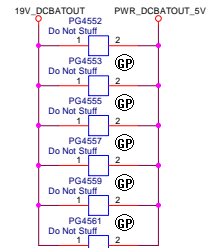
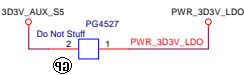
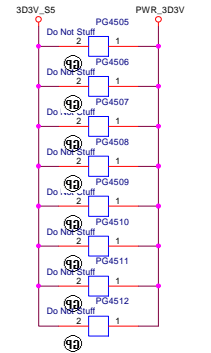
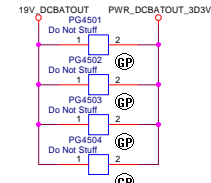
$$V_{PSYS} = R_{PSYS} \times K_{PSYS} (V_{ACP} \times I_{IN} + V_{BAT} \times I_{BAT}) \quad PWR$$



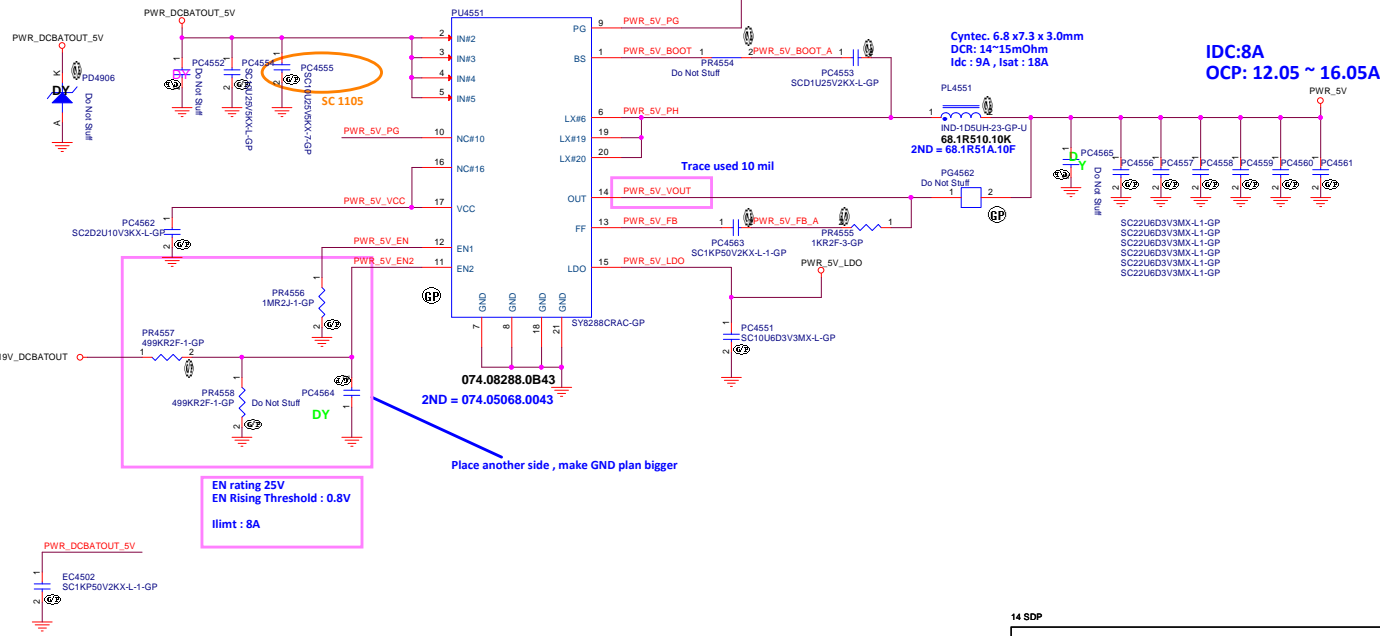
## OFFPAGE-Signal



## OFFPAGE-GAP



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14 SDP

緯創資通 Wistron Corporation	
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File	SY8288C&SY8288B_5V3D3V
Size	Document Number
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Date: Thursday, November 05, 2020	Sheet 45 of 100
	SB

```
{47} PWR_VCORE_FCCM  <<-----
{47} PWR_VCORE_ISUMP >>-----
{47} PWR_VCORE_ISUMN_A >>-----
```

{47}	PWR_VCORE_ISEN1	»»	_____
{47}	PWR_VCORE_ISEN2	»»	_____
{47}	PWR_VCORE_ISEN3	»»	_____
{47}	PWR_VCORE_ISEN4	»»	_____

```
{47} PWR_VCORE_PWM1 <<—————
{47} PWR_VCORE_PWM2 <<—————
{47} PWR_VCORE_PWM3 <<—————
{47} PWR_VCORE_PWM4 <<—————
```

```

(8) PWR_VCORE_PWM_SOC <<-----
(8) PWR_VCORE_FCCM_SOC <<-----
(8) PWR_VCORE_VO_SOC >>-----
(8) PWR_VCORE_ISUMP_SOC >>-----

```

24,44,72}	PROCHOT#_CPU	◀
{24,40}	ALL_SYS_PWRGD	▶

(8) VDDNB\_SENSE >>————

(8) VCCCORE\_SENSE >> \_\_\_\_\_

(8) VSSCORE\_SENSE >> \_\_\_\_\_

SVID\_PWRGD 1 PR4617 2 PWR\_VCORE\_SVID\_PG  
Do Not Stuff

3D3V\_S0

VCORE\_PWRGD 1 PR4629 2 PWR\_VCORE\_PGOOD

4,26} VCORE\_PWRGD &lt;&lt;—————



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緯創資通

**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

### Block Diagram

Size

2

Date: Thursday, November 05, 2020

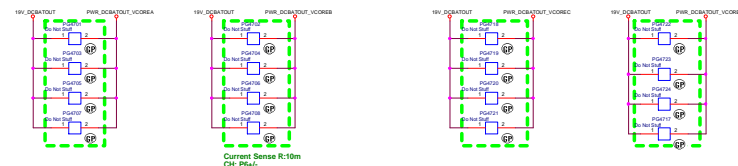
**55**

Rev

re

# OFFPAGE

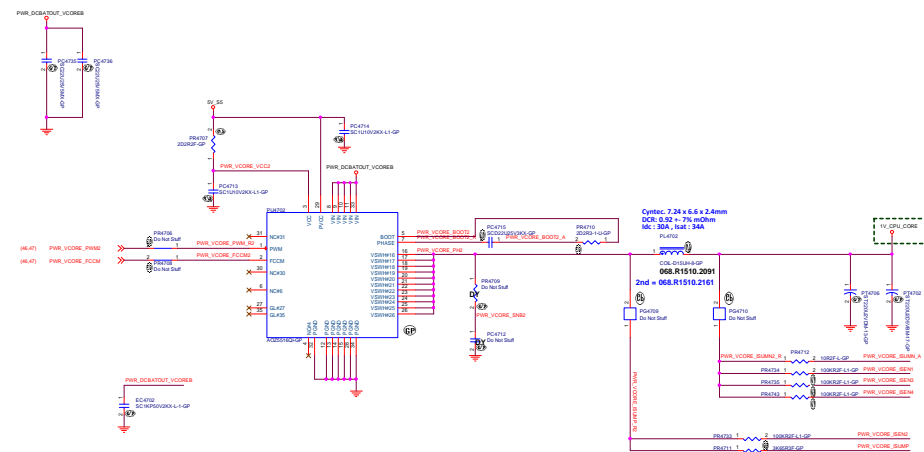
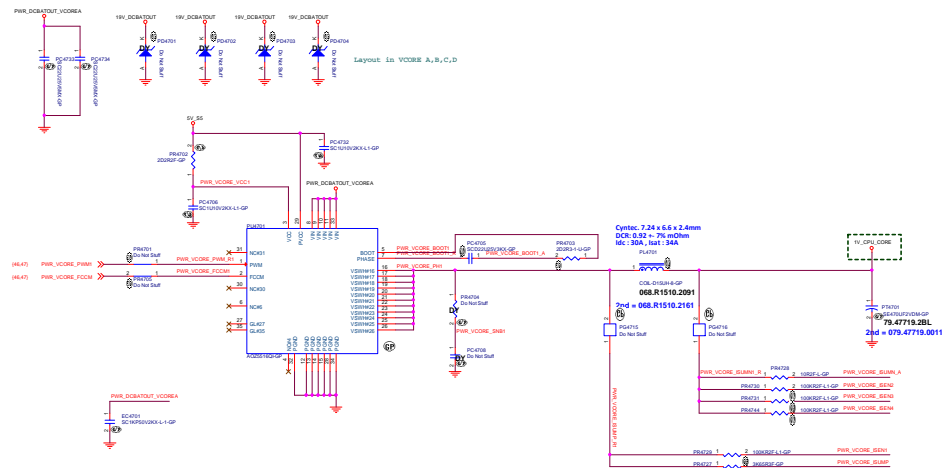
(H47) PWR\_VCORE\_FCCM  
 (H4) PWR\_VCORE\_SAMP  
 (H4) PWR\_VCORE\_SAMP\_A  
 (H4) PWR\_VCORE\_SEN1  
 (H4) PWR\_VCORE\_SEN2  
 (H4) PWR\_VCORE\_SEN3



## PHASE1

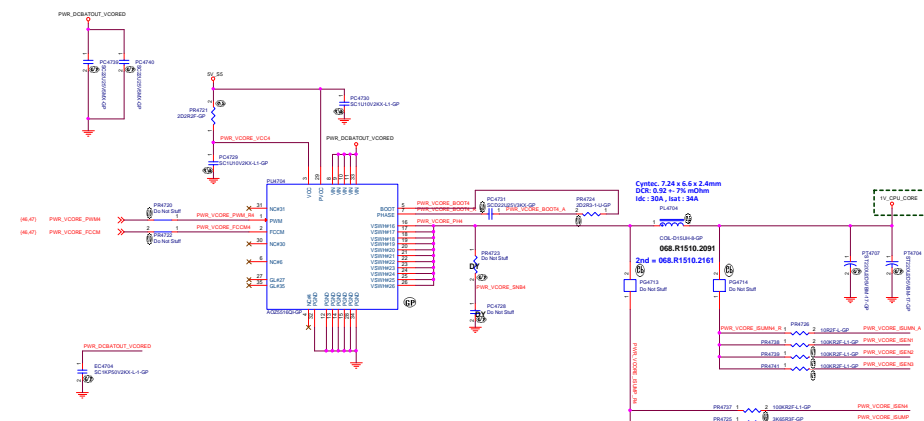
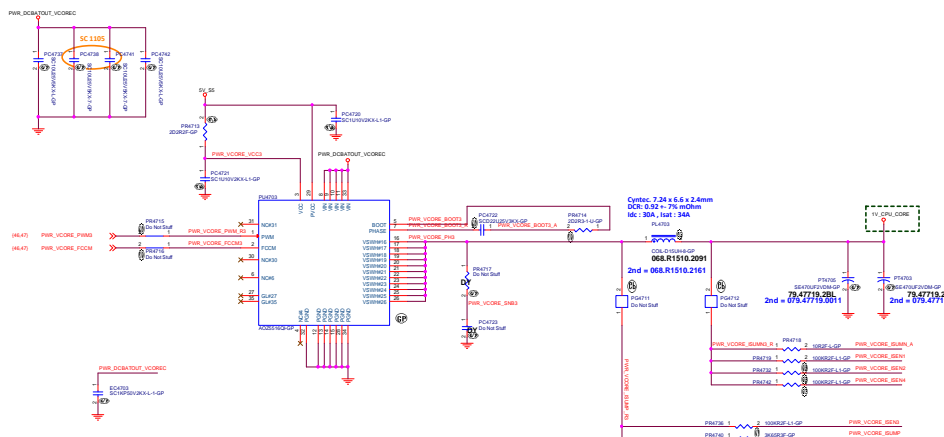
FP6 45W  
 TDC=58A  
 EDC=110A  
 132A<OCP<154A

## PHASE2

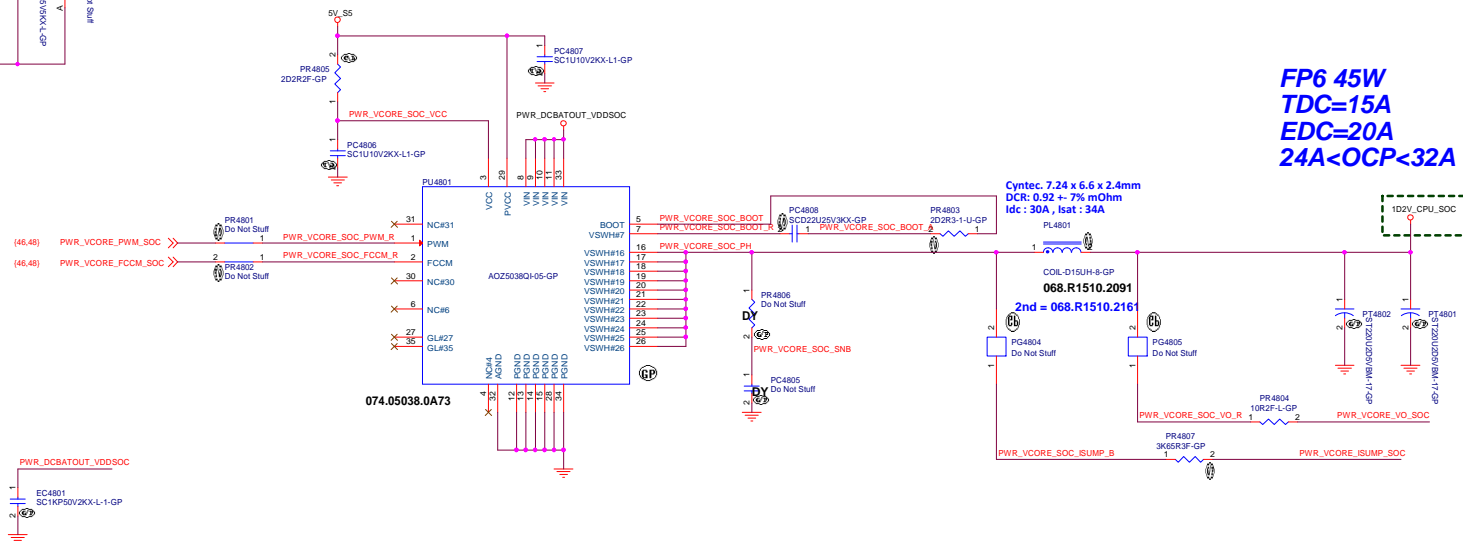
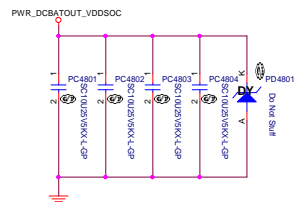


## PHASE3

## PHASE4



```
(46,48) PWR_VCORE_PWM_SOC >>-----
(46,48) PWR_VCORE_FCCM_SOC >>-----
(46) PWR_VCORE_VO_SOC <<-----
(46) PWR_VCORE_ISUMP_SOC <<-----
```



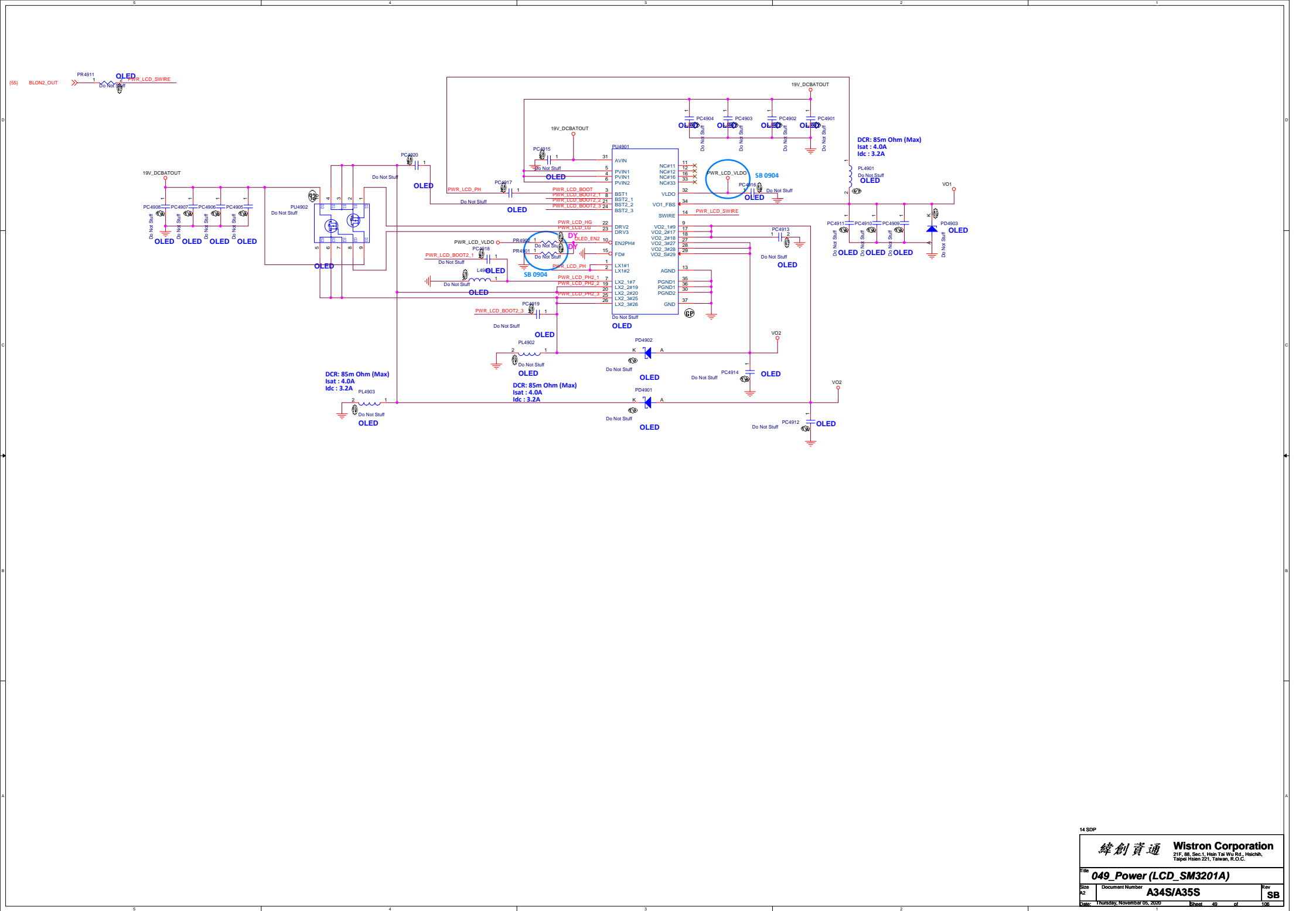
**FP6 45W**  
**TDC=15A**  
**EDC=20A**  
**24A<OCP<32A**

14 SDP

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien Z21, Taiwan, R.O.C.

Title	<b>BQ24781R_Charger</b>
-------	-------------------------

Size A2	Document Number <b>A34S/A35S</b>	Rev <b>SB</b>
Date: Thursday, November 05, 2020	Sheet 48 of	106



5	4	3	2	1
D				D
C				C
B				B
A			14 SDP	A
			<div><div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div><div><div>Title</div><div>Reserved</div></div><div><div><div>Size</div><div>A</div></div><div><div>Document Number</div><div>A34S/A35S</div></div><div><div>Rev</div><div>SB</div></div></div><div><div>Date:</div><div>Thursday, November 05, 2020</div><div>Sheet</div><div>50</div><div>of</div><div>106</div></div></div>	
5	4	3	2	1

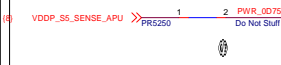


# OFFPAGE-Signal

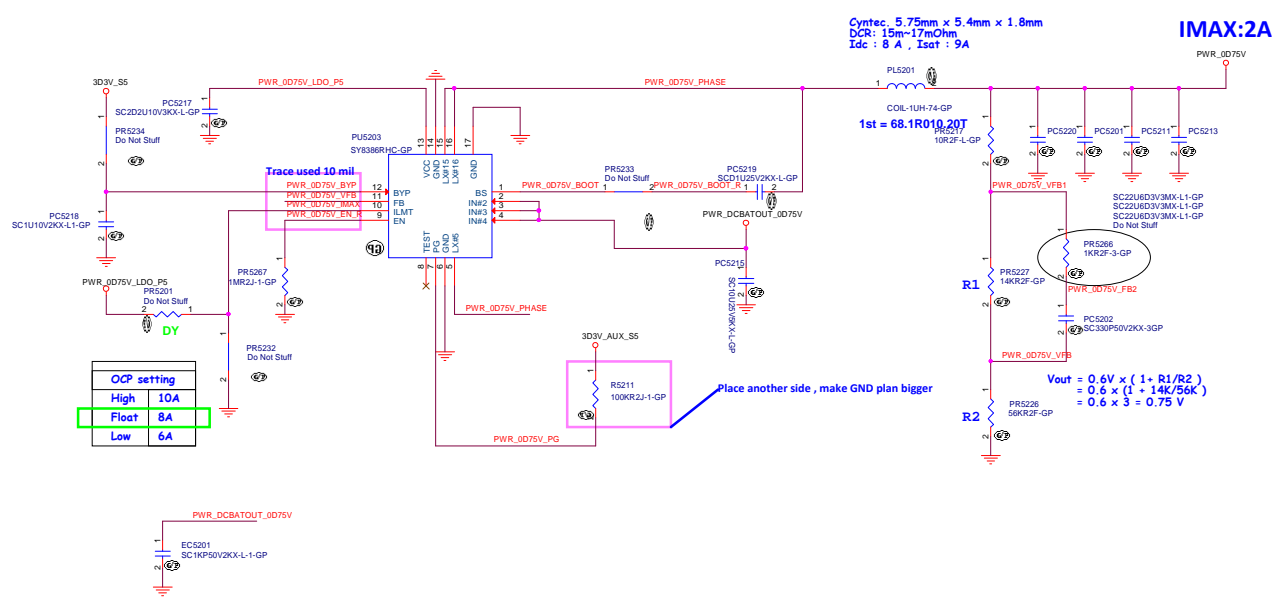
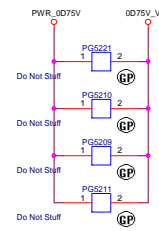
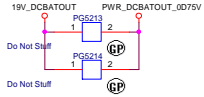


PWR\_0D75V\_PG

Closing PWR



# OFFPAGE-GAP



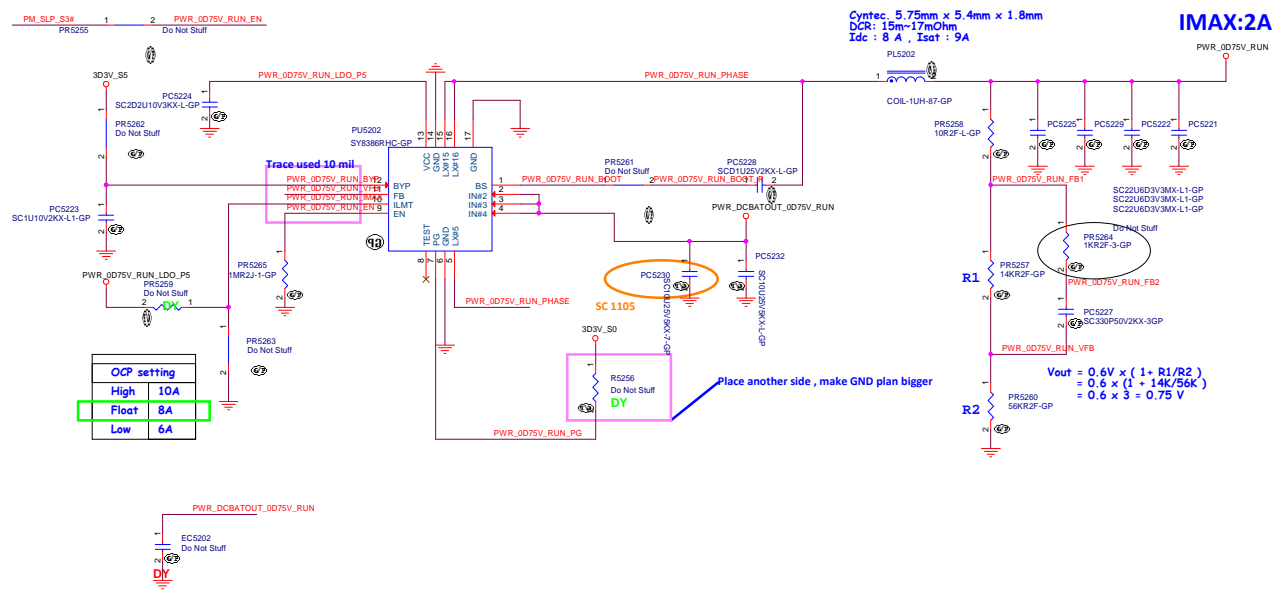
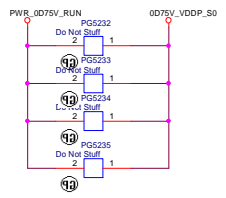
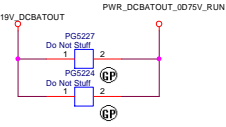
# OFFPAGE-Signal

PM\_SLP\_S3#

Closing PWR



# OFFPAGE-GAP





[illegible][illegible][illegible]

**OFFPAGE**

(52) PWR\_0D75V\_PG >> PWR\_1D8V\_EN  
OR2J-2-GP

(45) PWR\_1D8V\_PG << PWR\_1D8V\_PG

**OFFPAGE\_GAP**

19V\_DCBATOUT PG5301 Do Not Shift  
PG5302 Do Not Shift  
PG5303 Do Not Shift

PWR\_DCBATOUT\_1D8V

PWR\_1D8V 1D8V\_S5

PG5304 Do Not Shift  
PG5305 Do Not Shift  
PG5316 Do Not Shift  
PG5320 Do Not Shift  
PG5321 Do Not Shift  
PG5322 Do Not Shift

1D8V\_PWR 1D8V\_AUX\_S5 1D8V\_S5

R5309 R5305  
OR5J-L1-GP Do Not Shift  
**R5306 , R5309 On BOT**

**SSID = PWR.Plane.Regulator\_1p0v**

1D8V\_S5 SB 0805  
PR5308 100KR2J-4-GP  
PWR\_1D8V\_PG

PWR\_DCBATOUT\_1D8V EC5301 SC1KP50V2KX-L-1-GP

PWR\_DCBATOUT\_1D8V PC5304 4D7XX06/G2T1UCS  
PC5315 SC 1105  
PC5302 SC1U0R03VMXL-GP

**RT9078-18GJ5 for 1D8V\_AUX\_S5**

3D3V\_AUX\_S5O R5306 OR2J-2-GP  
C5309 SC1U10V2KX-1-GP

1D8V\_PWR\_VIN 1D8V\_AUX\_EN VIN GND EN SNS/NC/RA  
US51 RT9078-18GJ5-GP 074.09078.003F

C5304 Do Not Shift  
C5308 SC1U10V2KX-1-GP

**G5335D for 1D8V**

5V\_S5

PLUS301 VCC LXI24 LXI18 LXI17 LXI16 LXI15 LXI14 LXI13 LXI12 LXI11 LXI10 BST FB AGND PGND PGND PGND PGND PGND PGND

PWR\_1D8V\_TON PWR\_1D8V\_PG PWR\_1D8V\_EN PWR\_1D8V\_PFM PWR\_1D8V\_SS

PR5303 4D7CT-J20N001  
PC5313 4D7TY-X06/G2T1UCS

PL5301 PWR\_1D8V\_PH COIL-1UH-34-GP-U1 68.1R01A.20B 2nd = 68.1R01B.10K  
PWR\_1D8V\_BT PWR\_1D8V\_VFB

Cyntec . 6.8mm x 7.3mm x 3.0mm  
DCR:10mOhm  
Idc : 12 A , Isat : 22A

I<sub>max</sub>=3.7A

PC5301 PC5302 PC5303 PC5304 PC5305 PC5306  
Do Not Shift DY DY DY DY DY

SC22U6D3VMXL-L1-GP SC22U6D3VMXL-L1-GP  
Do Not Shift Do Not Shift Do Not Shift Do Not Shift

PWR\_1D8V\_VFB\_A

PR5302 12K7R2F-GP  
PR5304 10KR2F-L1-GP  
DY  
PC5312 JPS/SNS/CQ

V<sub>O</sub>=0.8x(1+R1/R2)  
=0.8x(1+12.7/10)  
=1.816

**14 SDP**


<b>緯創資通 Wistron Corporation</b>	
21F, 6B, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.	
Title <b>G5335D 1D8V</b>	
Size Custom	Document Number <b>A34S/A35S</b>
Date Thursday, November 05, 2020	Sheet 53 of 106

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Title <b>Power (RSVD)</b>			
Size A4	Document Number <b>A34S/A35S</b>		Rev <b>SB</b>
Date: Thursday, November 05, 2020		Sheet 54 of	106

# Main Func = LCD

(8) eDP\_TX\_CPU\_N0  
(8) eDP\_TX\_CPU\_P0  
(8) eDP\_TX\_CPU\_N1  
(8) eDP\_TX\_CPU\_P1  
(8) eDP\_TX\_CPU\_N2  
(8) eDP\_TX\_CPU\_P2  
(8) eDP\_TX\_CPU\_N3  
(8) eDP\_TX\_CPU\_P3

(8) eDP\_AUX\_CPU\_N  
(8) eDP\_AUX\_CPU\_P  
(8) eDP\_HPD\_CPU  
(8) eDP\_VDDEN\_CPU  
(8) eDP\_VARY\_BL

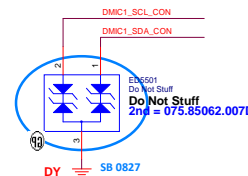
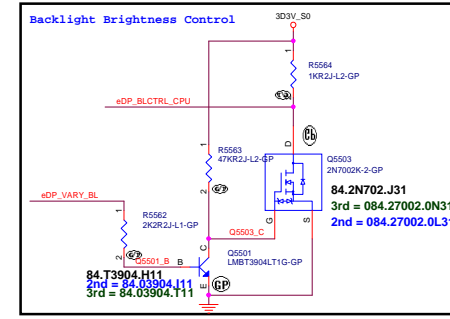
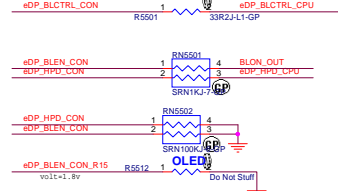
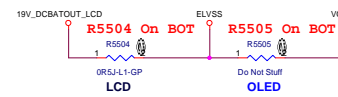
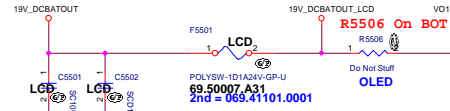
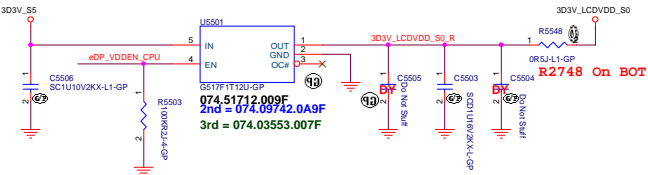
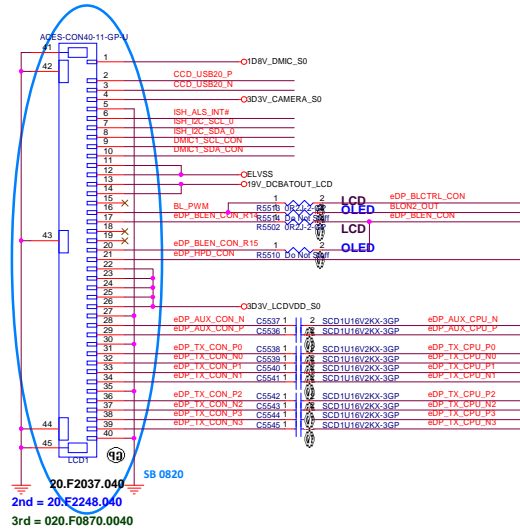
(24) BLON\_OUT  
(8) eDP\_BLCtrl\_CON  
(8) eDP\_BLEN\_CON  
(8) eDP\_HPD\_CON  
(17) ISH\_IC\_SCL\_0  
(17) ISH\_IC\_SDA\_0

(49) BLON2\_OUT

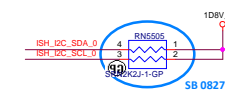
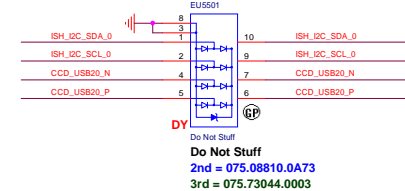
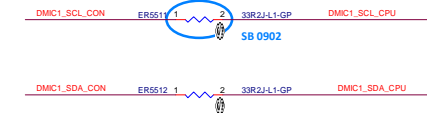
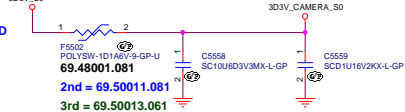
(17) ISH\_ALS\_INT#

(17) DMIC1\_SCL\_CPU  
(17) DMIC1\_SDA\_CPU

(18) CCD\_USB20\_N  
(18) CCD\_USB20\_P



## Camera Power



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Title <div>Display (RSVD)</div>		
Size <div>A4</div>	Document Number <div>A34S/A35S</div>	Rev <div>SB</div>
Date <div>Thursday, November 05, 2020</div>		Sheet <div>56</div> of <div>106</div>

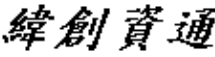


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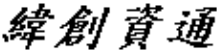
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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Display (HDMI/Conn)</b>			
Size A4	Document Number <b>A34S/A35S</b>		Rev <b>SB</b>
Date: Thursday, November 05, 2020		Sheet 57	of 106

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Title <b>Display (HDMI Power)</b>			
Size A4	Document Number <b>A34S/A35S</b>		Rev <b>SB</b>
Date: Thursday, November 05, 2020		Sheet 58 of	106

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Title **Display (RSVD)**

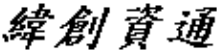
Size A4	Document Number <b>A34S/A35S</b>	Rev <b>SB</b>
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Date: Thursday, November 05, 2020 Sheet 59 of 106

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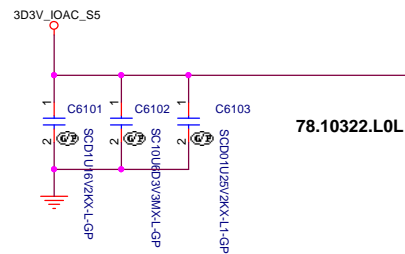
14 SDP

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>INT IO (RSVD)</b>			
Size A4	Document Number <b>A34S/A35S</b>		Rev <b>SB</b>
Date: Thursday, November 05, 2020		Sheet 60 of	106



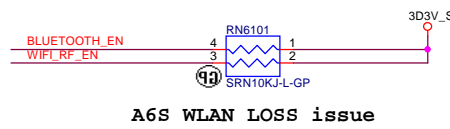
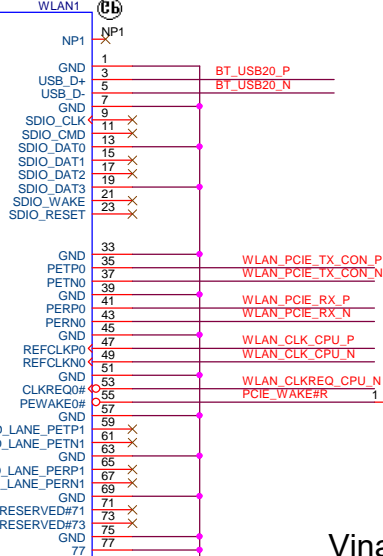
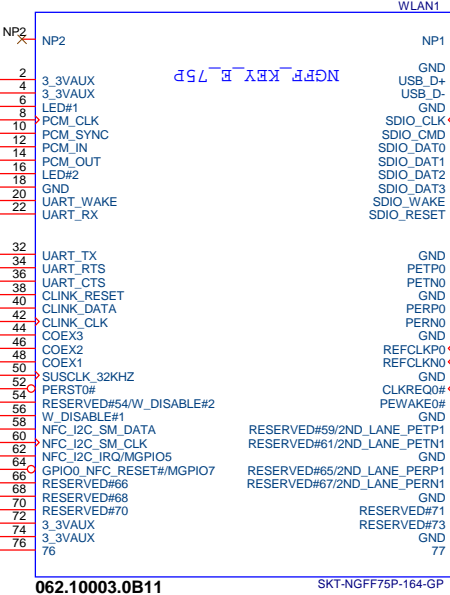
# SSID = Wireless Mini Card Connector(802.11a/b/g/n)

- (24,68) E51\_TXD >>>
- (18) BT\_USB20\_N >>>
- (18) BT\_USB20\_P >>>
- (17,63,68,72,89,92) PLT\_RST# >>>
- (24,89) BLUETOOTH\_EN >>>
- (24,89) WIFI\_RF\_EN >>>
- (3) WLAN\_PCIE\_TX\_CON\_P >>>
- (3) WLAN\_PCIE\_TX\_CON\_N >>>
- (3) WLAN\_PCIE\_RX\_P >>>
- (3) WLAN\_PCIE\_RX\_N >>>
- (16) WLAN\_CLK\_CPU\_P >>>
- (16) WLAN\_CLK\_CPU\_N >>>
- (16) WLAN\_CLKREQ\_CPU\_N >>>
- (17,63,89) PCIE\_WAKE# <<<
- (24) WLAN\_RST# <<<



Layout in BOT

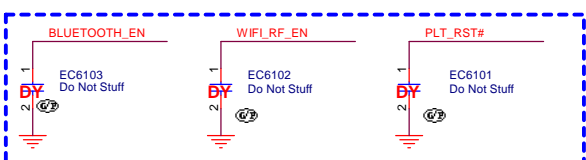
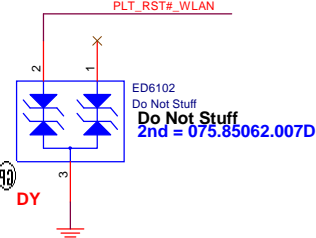
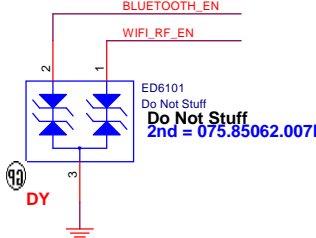
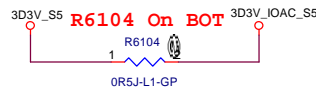
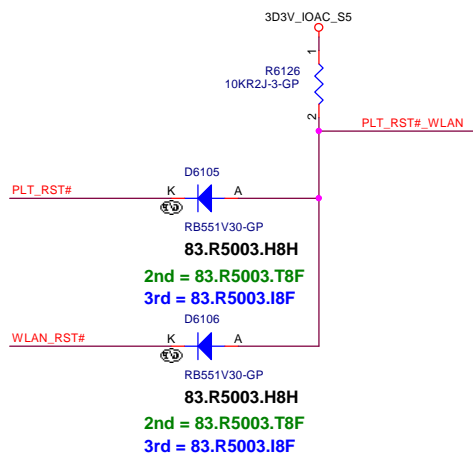
Clock route length = L	Recommended capacitor values
L < 5"	4.7pF
5" < L < 9"	2.2pF to 3.3pF
9" < L < 10"	1.0pF to 2.2pF



A6S WLAN LOSS issue

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## Modern Standby CIRCUIT



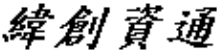
14 SDP

緯創資通 Wistron Corporation		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title INT IO (HDD)			
Size A3	Document Number A34S/A35S	Rev SB	
Date: Thursday, November 05, 2020	Sheet 61	of 106	

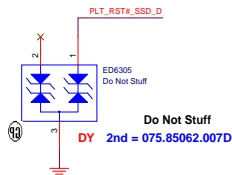
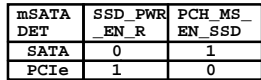
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Title <b>INT IO (RSVD)</b>			
Size A4	Document Number <b>A34S/A35S</b>		Rev <b>SB</b>
Date: Thursday, November 05, 2020		Sheet 62 of	106

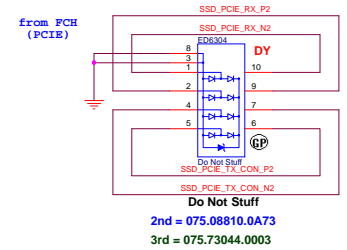
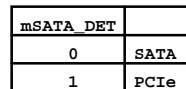
### Modern Standby CIRCUIT



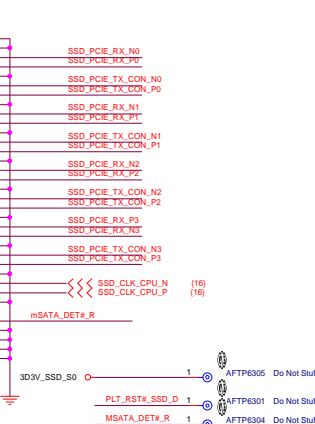


Function Table

INPUTS		OUTPUT Y
A	B	
H	H	H
L	X	L
X	L	L



		SSD	
5A	2	05C_W3X72_0000	GND
	3	3_VAUXV	GND
	4	3_VAUXV	D_PETP3M_PETP3
	5	N2C6	D_PETN3M_PETN3
	6	N2C8	D_PERN3M_PERN3
	7	DASQSS#	D_PERP3M_PETP3
	8	N2C6	GND
	9	3_VAUXV	D_PETN2M_PERN2
	10	N2C8	GND
	11	3_VAUXV	D_PETN2M_PERN2
	12	N2C6	GND
	13	N2C2	D_PERN2M_PETN2
	14	N2C6	D_PERP2M_PETP2
	15	N2C8	GND
	16	N2C2	D_PETN1M_PERN1
	17	N2C6	D_PET1M_PEP1
	18	N2C2	GND
	19	N2C34	D_PERN1M_PETN1
	20	N2C34	D_PERP1M_PETP1
	21	DEVSLP	GND
	22	N2C34	D_PETN0SATA_B,H,I,M,PERP0
	23	N2C42	D_PETP0SATA_B,H,I,M,PERP0
	24	N2C42	GND
	25	N2C46	D_PERN0SATA_A,B,H,I,M,PERN0
	26	N2C46	D_PERP0SATA_A,B,H,I,M,PERP0
	27	N2C48	GND
	28	PERP1M_PETN1C650	REFLCLK
	29	CLKREQ#N1C652	REFLCLK
	30	PERN1M_PETN1C654	REFLCLK
	31	N2C56	GND
	32	N2C58	SADET
	33	SUSCLK_32KHZ	NC667
	34	N2C62	PAETI/GND
	35	N2C62	GND
	36	3_VAUXV	GND
	37	3_VAUXV	GND
	38	3_VAUXV	GND
	39	N2C72	GND
	40	N2C72	GND
	41	N2C72	GND
	42	N2C72	GND
	43	N2C72	GND
	44	N2C72	GND
	45	N2C72	GND
	46	N2C72	GND
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	100	N2C72	GND
	101	N2C72	GND
	102	N2C72	GND
	103	N2C72	GND
	104	N2C72	GND
	105	N2C72	GND
	106	N2C72	



74	3.3V	GND	75
72	3.3V	GND	73
70		GND	71
68	SUSCLK(30KHz) (O)(0/3.3V)	PEDET (NC-PCIe/GND-SATA)	69
	Connector Key	N/C	67
	Connector Key	Connector Key	



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14 SDP

緯創資通

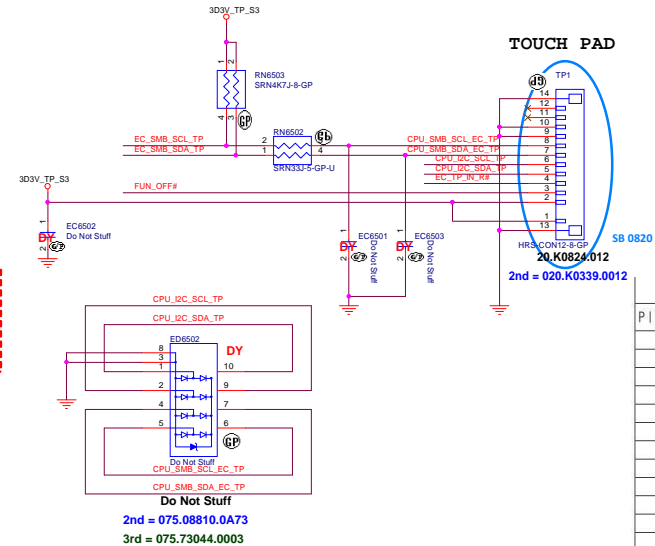
**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title **LED / Button / Power Button**

Size A4	Document Number <b>A34S/A35S</b>	Rev <b>SB</b>
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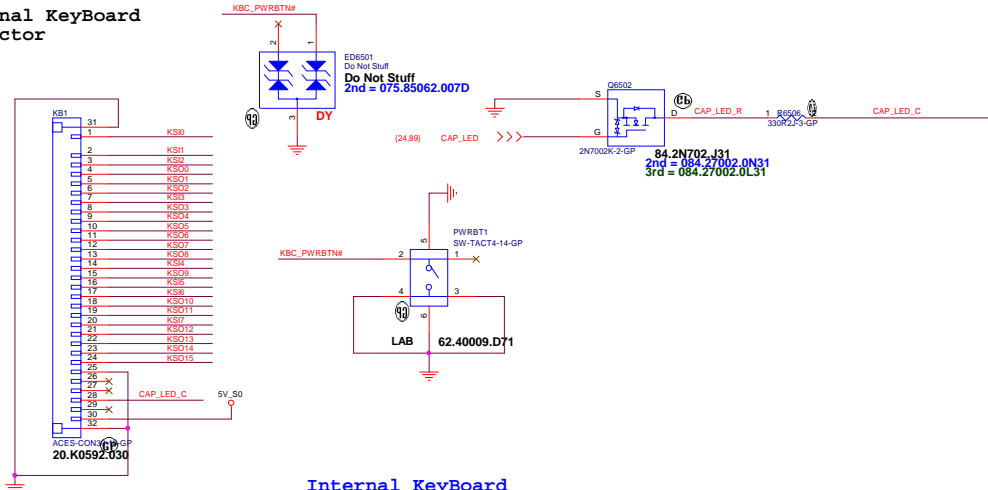
Date: Thursday, November 05, 2020	Sheet 64 of 106
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(17)	CPU_I2C_SCL_P3	↔
(17)	CPU_I2C_SDA_P3	↔
(17)	TP_IN#	↔
(24)	EC_TP_IN#	↔
(24)	PTT_PWR_EN	↔
(24)	EC_SMB_SCL_TP	↔
(24)	EC_SMB_SDA_TP	↔
(24,89)	FUN_OFF#	↔
(89)	CPU_SMB_SCL_EC_TP	↔
(89)	CPU_SMB_SDA_EC_TP	↔
(89)	CPU_I2C_SDA_TP	↔
(89)	CPU_I2C_SCL_TP	↔
(89)	EC_TP_IN_R#	↔
(24)	KD_PL_RST	↔



CNI	
PIN NO.	PIN DEFINE*
1	NC
2	NC
3	GND
4	GND
5	PS/2_CLK
6	PS/2_DATA
7	SCL
8	SDA
9	INT
10	LID_CLOSE
11	VDD_3.3V
12	VDD_3.3V

[24,89)	KS[0..7]	>>>
[24,89)	KSO[0..15]	<<<
[89,92)	KBC_PWRSTN#	<<<
[24)	KB_BL_PWM	>>>

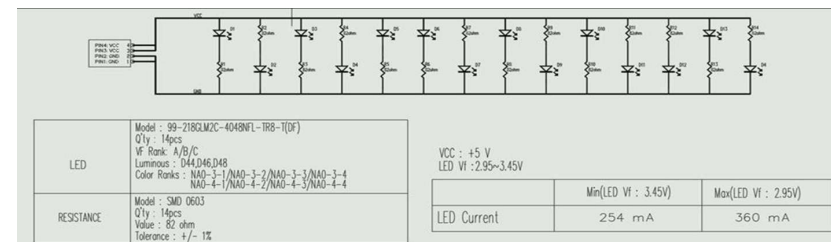
[illegible]

BackLight	
Pin4	P5V0S
Pin3	P5V0S
Pin2	GND
Pin1	GND

Membrane	
Pin1	SCAN_IN<0>
Pin2	SCAN_IN<1>
Pin3	SCAN_IN<2>
Pin4	SCAN_OUT<0>
Pin5	SCAN_OUT<1>
Pin6	SCAN_OUT<2>
Pin7	SCAN_IN<3>
Pin8	SCAN_OUT<3>
Pin9	SCAN_OUT<4>
Pin10	SCAN_OUT<5>
Pin11	SCAN_OUT<6>
Pin12	SCAN_OUT<7>
Pin13	SCAN_OUT<8>
Pin14	SCAN_IN<4>
Pin15	SCAN_OUT<9>
Pin16	SCAN_IN<5>
Pin17	SCAN_IN<6>
Pin18	SCAN_OUT<10>
Pin19	SCAN_OUT<11>
Pin20	SCAN_IN<7>
Pin21	SCAN_OUT<12>
Pin22	SCAN_OUT<13>
Pin23	SCAN_OUT<14>
Pin24	SCAN_OUT<15>
Pin25	N.C.
Pin26	N.C.
Pin27	N.C.
Pin28	CAPS_LED#_3
Pin29	N.C.
Pin30	P5V0S_CAPS

B/L FPC	
Pin Define	
PIN4	VCC
PIN3	VCC
PIN2	GND
PIN1	GND

MEM Keyboard Pin Define	
PIN 1	SCAN_IN<0>
PIN 2	SCAN_IN<1>
PIN 3	SCAN_IN<2>
PIN 4	SCAN_OUT<15>
PIN 5	SCAN_OUT<14>
PIN 6	SCAN_OUT<13>
PIN 7	SCAN_IN<3>
PIN 8	SCAN_OUT<12>
PIN 9	SCAN_OUT<11>
PIN 10	SCAN_OUT<10>
PIN 11	SCAN_OUT<9>
PIN 12	SCAN_OUT<8>
PIN 13	SCAN_OUT<7>
PIN 14	SCAN_IN<4>
PIN 15	SCAN_OUT<6>
PIN 16	SCAN_IN<5>
PIN 17	SCAN_IN<6>
PIN 18	SCAN_OUT<5>
PIN 19	SCAN_OUT<4>
PIN 20	SCAN_IN<7>
PIN 21	SCAN_OUT<3>
PIN 22	SCAN_OUT<2>
PIN 23	SCAN_OUT<1>
PIN 24	SCAN_OUT<0>
PIN 25	NC
PIN 26	NC
PIN 27	NC
PIN 28	CAPS_LED#_3
PIN 29	NC
PIN 30	PSV05_CAPS



SSID = User.Interface

## Audio Jack

{18} USB3\_USB20\_N  
{18} USB3\_USB20\_P

{27,89} RING2  
{27} AUD\_HP1\_JACK\_L2  
{27,89} AUD\_HP1\_JD#  
{27} AUD\_HP1\_JACK\_R2  
{27,89} SELEEVE

{18} USB2\_USB30\_RX\_N  
{18} USB2\_USB30\_RX\_P  
{18} USB2\_USB30\_TX\_N  
{18} USB2\_USB30\_TX\_P

{24,89} LID\_CLOSE#

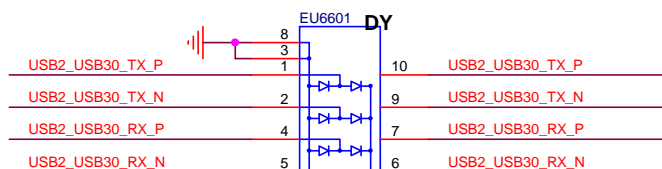
{72} USB2\_PD\_CC1  
{72} USB2\_PD\_CC2

{24,89} DC\_BATFULL

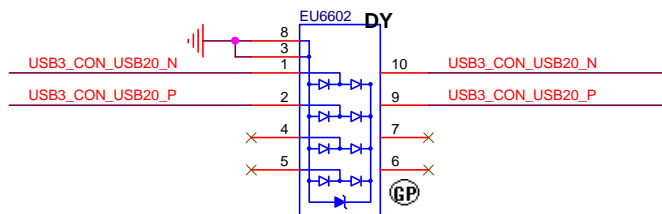
{24,89} CHARGE\_LED

{24,72} USB\_SEL

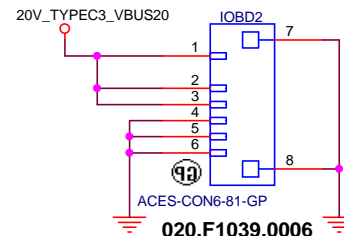
USB3\_USB20\_N R6601 1 0R2J-2-GP USB3\_CON\_USB20\_N  
USB3\_USB20\_P R6602 1 0R2J-2-GP USB3\_CON\_USB20\_P



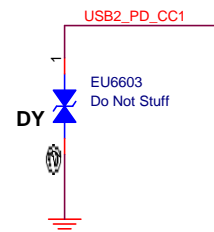
Do Not Stuff  
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3rd = 075.73044.0003



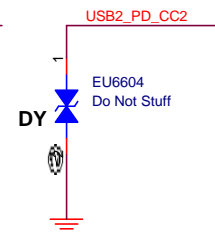
Do Not Stuff  
2nd = 075.08810.0A73  
3rd = 075.73044.0003



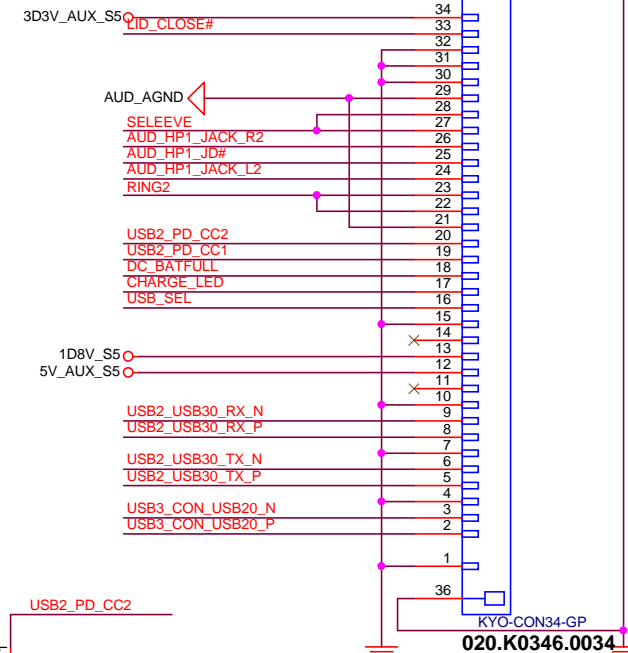
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DY



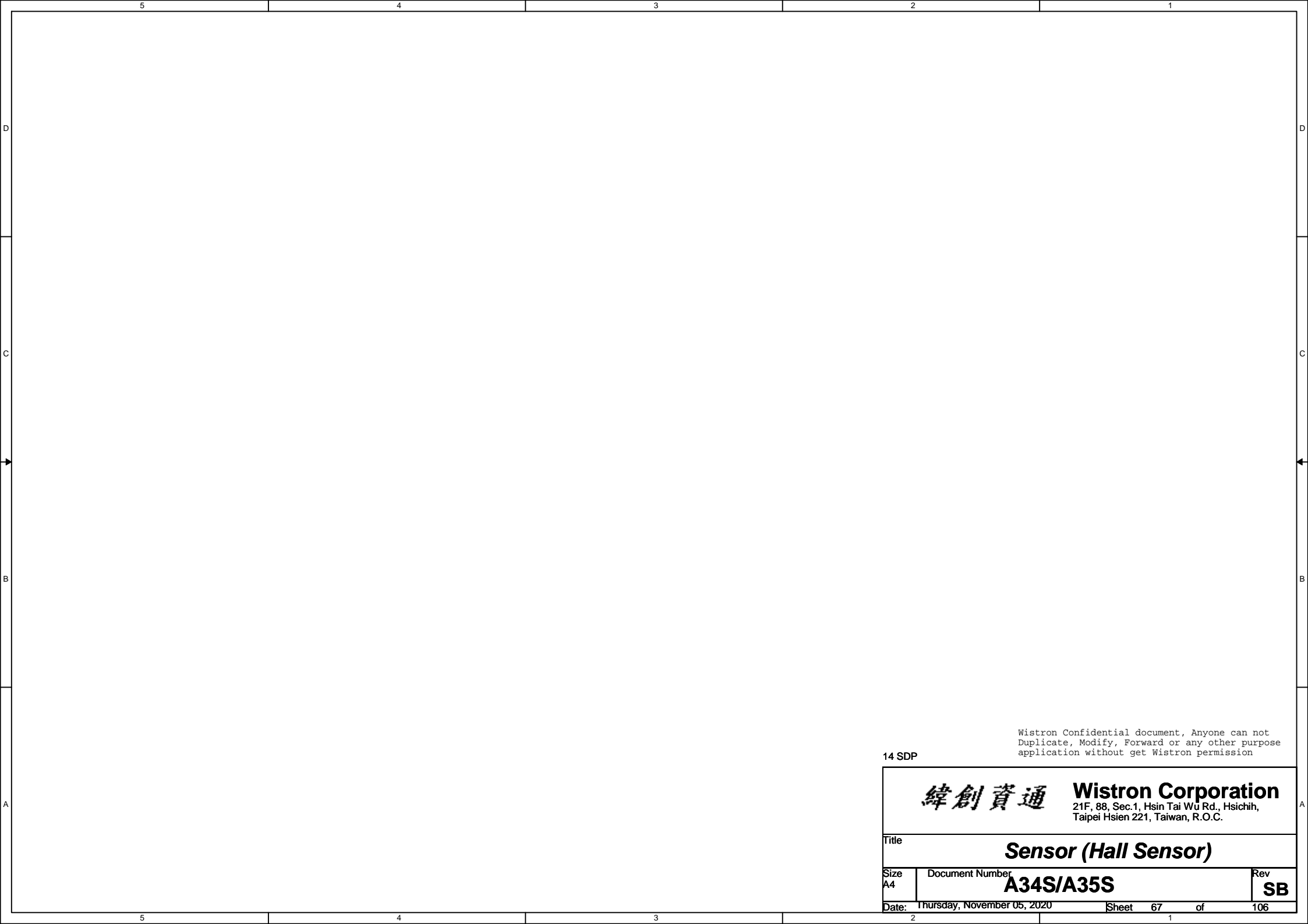
DY



2nd = 020.K0270.0034

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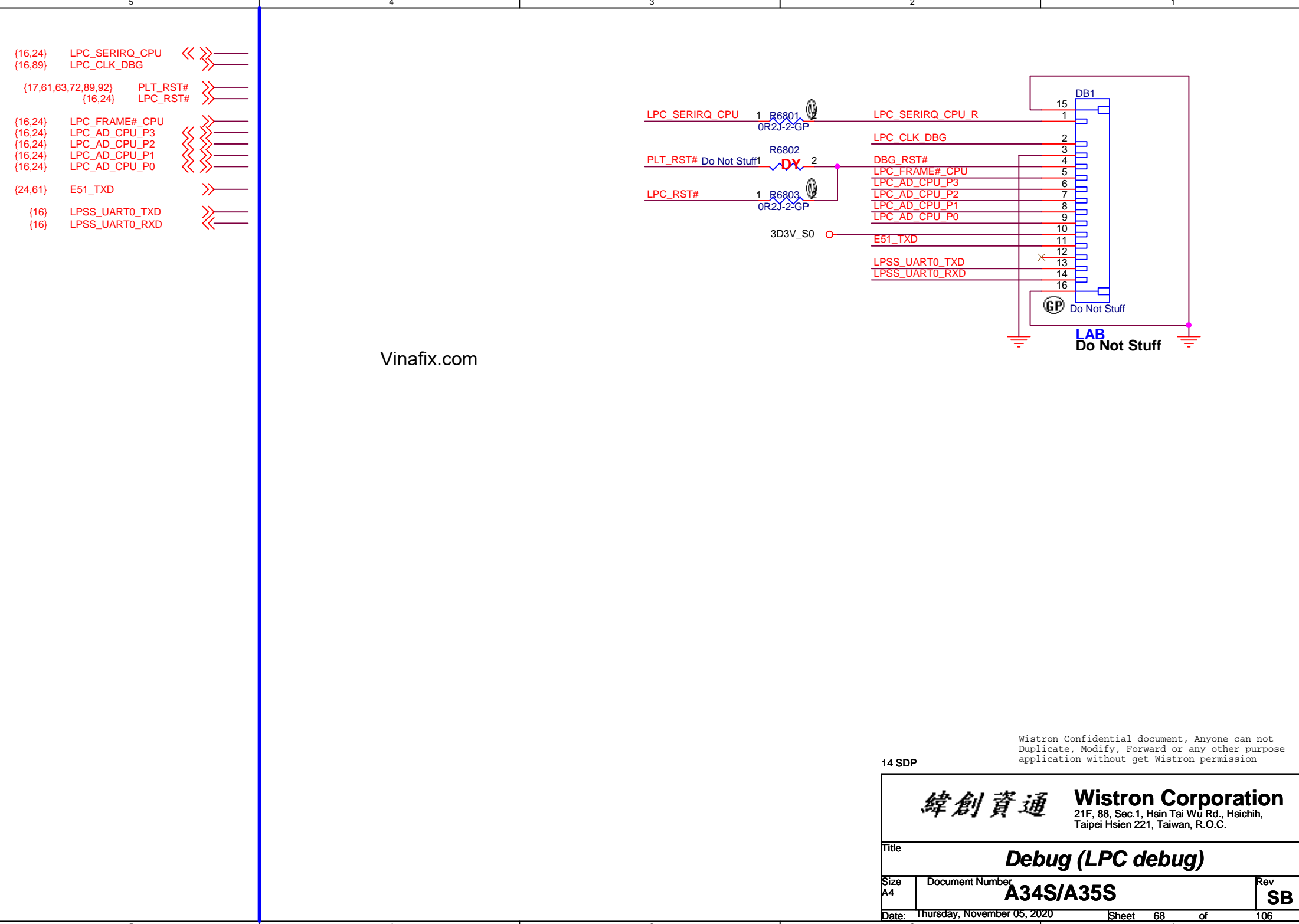
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Title IO Board Conn (USB/AUDIO)			
Size	Document Number	Rev	
Custom	A34S/A35S	SB	
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<div>緯創資通</div>		<div>Wistron Corporation</div>	
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Title			
<div>Sensor (Hall Sensor)</div>			
Size A4	Document Number A34S/A35S		Rev SB
Date:	Thursday, November 05, 2020		Sheet 67 of 106



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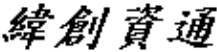
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Title			
Debug (LPC debug)			
Size	Document Number	Rev	
A4	A34S/A35S	SB	
Date:	Thursday, November 05, 2020	Sheet	68 of 106



# Blanking

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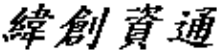
14 SDP

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Sensor (RSVD)</b>			
Size A4	Document Number <b>A34S/A35S</b>		Rev <b>SB</b>
Date: Thursday, November 05, 2020		Sheet 69 of	106

# Blanking

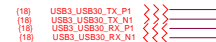
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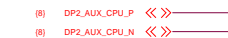
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Sensor (RSVD)</b>			
Size A4	Document Number <b>A34S/A35S</b>		Rev <b>SB</b>
Date: Thursday, November 05, 2020		Sheet 70 of	106

## Main Func = TYPEC MUX

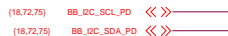
From CPU



## DisplayPort AUX



**MUX I2C**



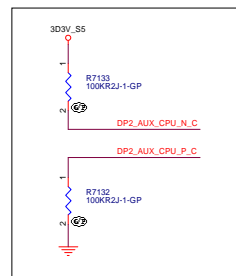
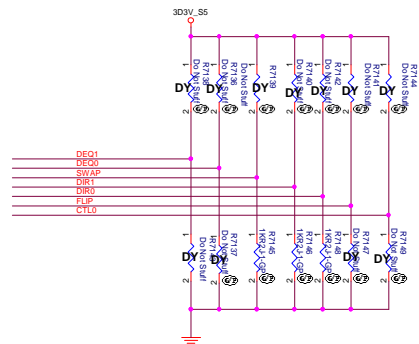
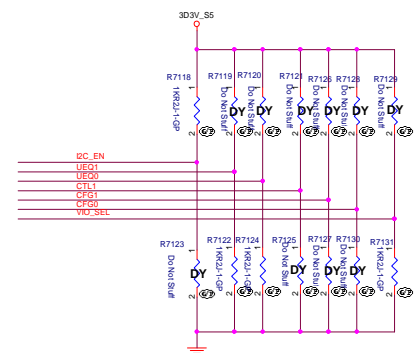
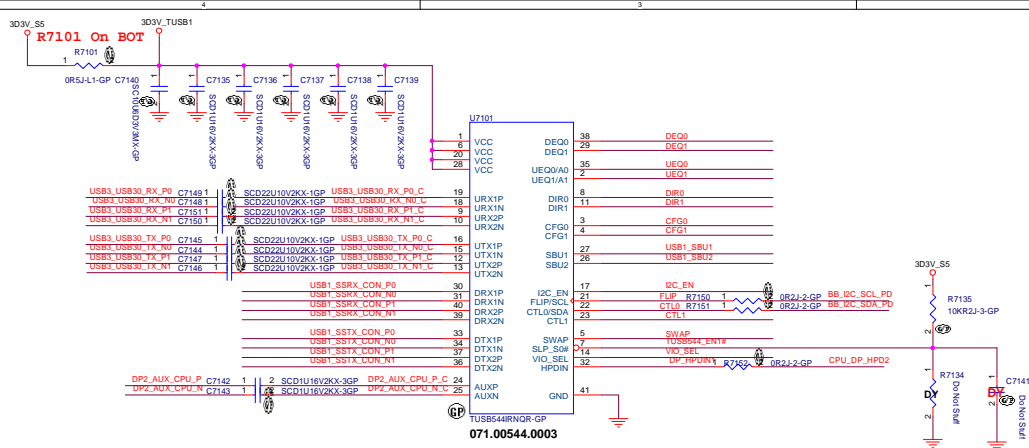
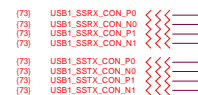
## Re-Driver ctrl



## HPD



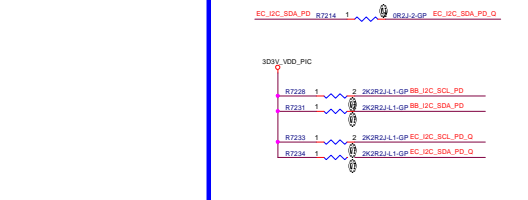
## I2C/USB MUX



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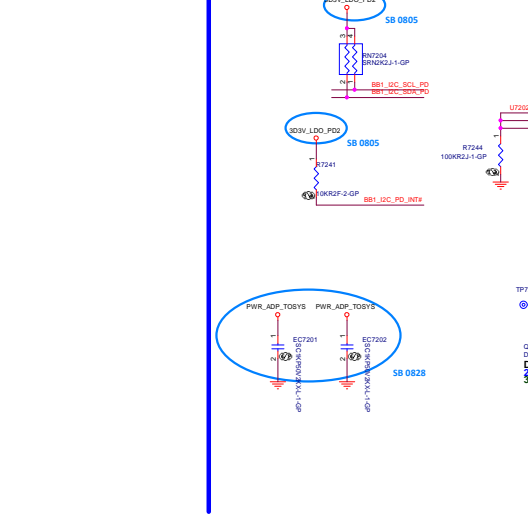
Main Func = TypeC

- (24) EC\_ICN\_INTP\_PD >>>
- (17) USB1\_PDA\_CCI >>>
- (17) USB1\_PDA\_CCI >>>
- (17) USB2\_PDA\_CCI >>>
- (17) USB2\_PDA\_CCI >>>
- (71) TUB844\_ENIN <<<
- (76) TUB844\_ENIN <<<
- (17,17,17) BB\_ICN\_INTP <<<
- (17,17,17) BB\_ICN\_INTP <<<
- (24) EC\_ICN\_SDA\_PD <<<
- (24) EC\_ICN\_SDA\_PD <<<
- (8,24,44,46) PROCHOTX\_CPU <<<
- (8,71) CPU\_DP\_HPD2 <<<
- (8,76) CPU\_DP\_HPD2 <<<
- (17,61,63,66,69,92) PLT\_RSTN <<<

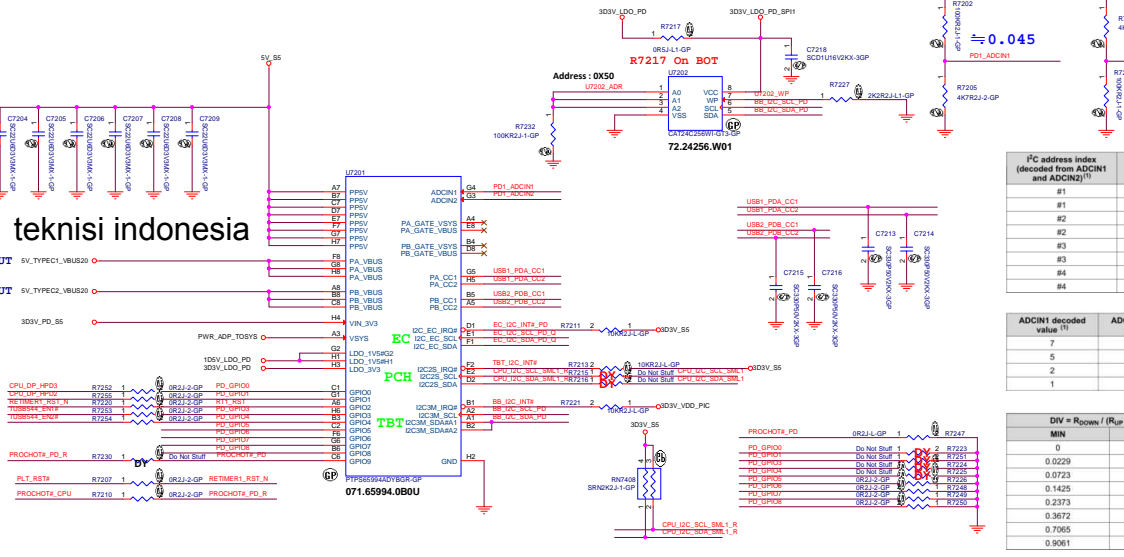


PD to EC/TP

- (24) EC\_ICN\_INTP\_PD <<<
- (24,66) USB\_SEL >>>
- (66) USB2\_PDA\_CCI >>>
- (66) USB2\_PDA\_CCI >>>



PD for TYPEC 1 (USBC) & TYPEC 2 (USBC)

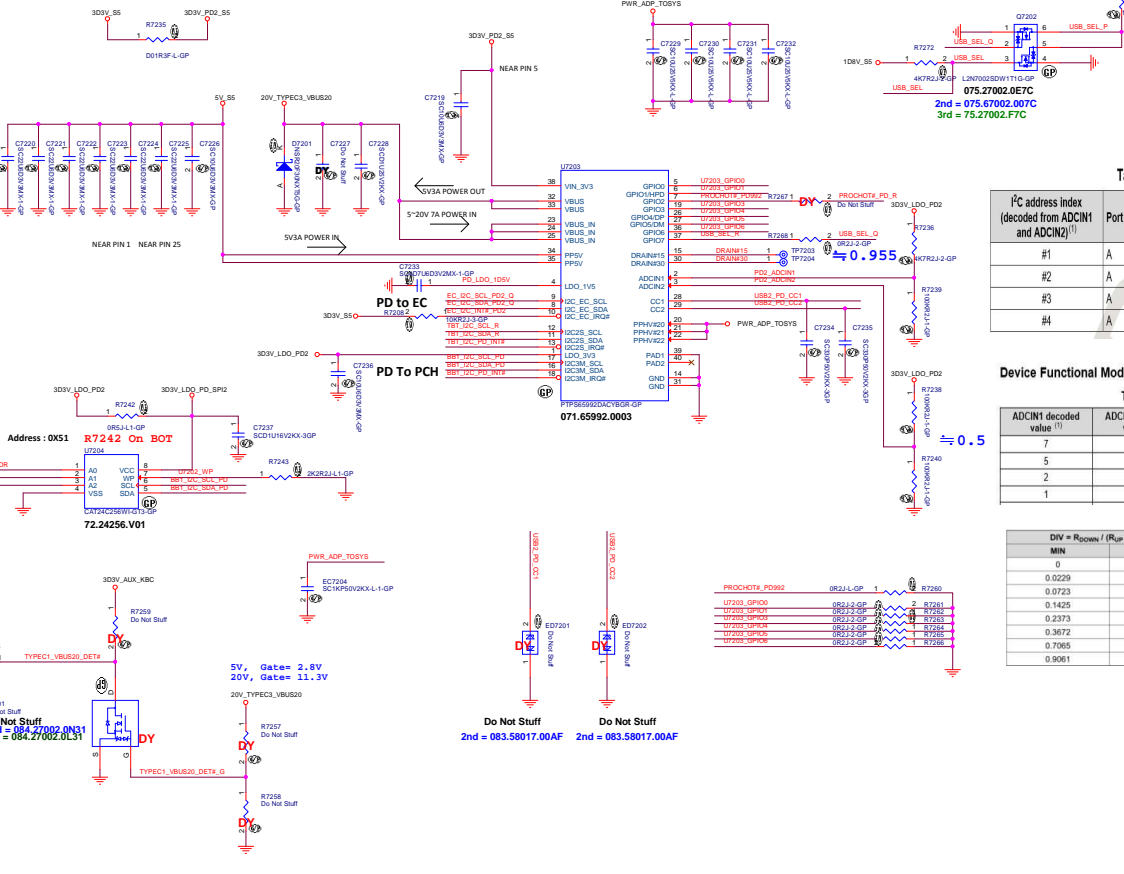


teknisi indonesia

Power OUT 5V,TYPEC1\_VBUS20

Power OUT 5V,TYPEC2\_VBUS20

PD for TYPEC BD(IO)



I2C Address Selection

I2C1 Master: EC	USB1(TB74)	0x23	TCPO
I2C1 Slave: PD	USB2	0x27	
I2C2 Master: CPU	USB1(TB74)	0x23	TCPO
I2C2 Slave: PD	USB2	0x27	
I2C3 Master: PD	USB1(TB74)	0x23	TCPO
I2C3 Slave: Retimer	USB2		

Table 5. I2C Default Slave Address for I2C\_EC\_SCL/SDA.

I <sup>2</sup> C address index (decoded from ADCIN1 and ADCIN2) <sup>(1)</sup>	Port	Slave Address								Available During BOOT
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
#1	A	0	1	0	0	0	0	0	R/W	Yes
#2	B	0	1	0	0	0	1	0	R/W	No
#3	A	0	1	0	0	0	0	1	R/W	Yes
#4	B	0	1	0	0	0	1	0	R/W	No
#5	A	0	1	0	0	0	1	1	R/W	Yes
#6	B	0	1	0	0	1	1	0	R/W	No
#7	A	0	1	0	0	1	0	1	R/W	Yes
#8	B	0	1	0	0	1	1	1	R/W	No

Table 6. Device Configuration using ADCIN1 and ADCIN2

ADCIN1 decoded value <sup>(1)</sup>	ADCIN2 decoded value <sup>(1)</sup>	I2C address index <sup>(2)</sup>	Dead Battery Configuration
7	5	#1	AlwaysEnableSink: The device always enables the sink path regardless of the amount of current the attached source is offering. USB PD is disabled until configuration is loaded.
5	5	#2	
2	0	#3	
1	7	#4	

Table 2. Decoding of ADCIN1 and ADCIN2 Pins

DIV = R <sub>DOWN</sub> / (R <sub>UP</sub> + R <sub>DOWN</sub> ) <sup>(1)</sup>		Without using R <sub>UP</sub> or R <sub>DOWN</sub>	ADCINx decoded value
MIN	MAX		
0	0.0228	tie to GND	0
0.0229	0.0722	N/A	1
0.0723	0.1425	N/A	2
0.1425	0.2372	N/A	3
0.2373	0.3671	N/A	4
0.3672	0.7054	tie to LDO_1V5	5
0.7055	0.9060	N/A	6
0.9061	1.0	tie to LDO_3V3	7

I2C Address Selection

I2C1 Master: EC	USB3(IO)	0x20
I2C1 Slave: PD	USB3(IO)	
I2C2 Master: CPU	USB3(IO)	0x20
I2C2 Slave: PD	USB3(IO)	
I2C3 Master: PD	USB3(IO)	
I2C3 Slave: ROM	USB3(IO)	

Table 5. I2C Default Slave Address for I2C\_EC\_SCL/SDA.

PC address index (decoded from ADCIN1 and ADCIN2) <sup>(1)</sup>	Port	Slave Address								Available During BOOT
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
#1	A	0	1	0	0	0	0	0	R/W	Yes
#2	A	0	1	0	0	0	0	1	R/W	Yes
#3	A	0	1	0	0	0	1	0	R/W	Yes
#4	A	0	1	0	0	0	1	1	R/W	Yes

Device Functional Modes (continued)

Table 6. Device Configuration using ADCIN1 and ADCIN2.

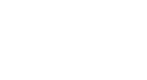
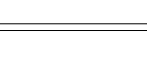
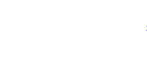
ADCIN1 decoded value <sup>(1)</sup>	ADCIN2 decoded value <sup>(1)</sup>	I2C address index <sup>(2)</sup>	Dead Battery Configuration
7	5	#1	AlwaysEnableSink: The device always enables the sink path regardless of the amount of current the attached source is offering. USB PD is disabled until configuration is loaded.
5	5	#2	
2	0	#3	
1	7	#4	

Table 2. Decoding of ADCIN1 and ADCIN2 Pins

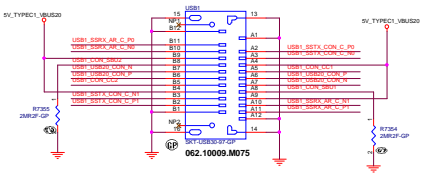
DIV = R <sub>DOWN</sub> / (R <sub>UP</sub> + R <sub>DOWN</sub> ) <sup>(1)</sup>		Without using R <sub>UP</sub> or R <sub>DOWN</sub>	ADCINx decoded value
MIN	MAX		
0	0.0228	tie to GND	0
0.0229	0.0722	N/A	1
0.0723	0.1425	N/A	2
0.1425	0.2372	N/A	3
0.2373	0.3671	N/A	4
0.3672	0.7054	tie to LDO_1V5	5
0.7055	0.9060	N/A	6
0.9061	1.0	tie to LDO_3V3	7

Main Form = TypeC

USB1

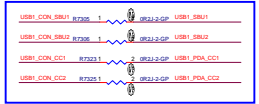


TYPE C CON.  
USB3.1 Gen1 / DP1.2

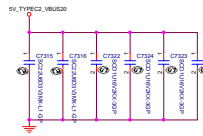
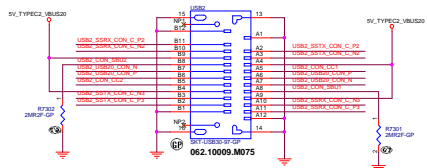


PIN	SIGNAL NAME	PIN	SIGNAL NAME
A1	GND	B12	GND
A2	SSTxp1	B11	SSRXp1
A3	SSTXn1	B10	SSRXn1
A4	VBUS	B9	VBUS
A5	CC1	B8	SBU2
A6	Dp1	B7	Dn2
A7	Dn1	B6	Dp2
A8	SBU1	B5	CC2
A9	VBUS	B4	VBUS
A10	SSRXn2	B3	SSTXn2
A11	SSRXp2	B2	SSTXp2
A12	GND	B1	GND

Co-lay with U7304

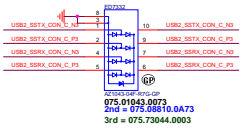
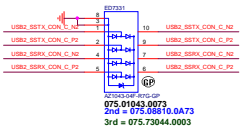
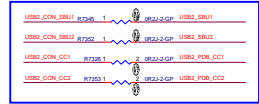


TYPE C CON.  
USB3.1 Gen1 / DP1.2



Pin	SIGNALNAME	Pin	SIGNAL NAME
A1	GND	B12	GND
A2	SSTxp1	B11	SSRXp1
A3	SSTXn1	B10	SSRXn1
A4	VBUS	B9	VBUS
A5	CC1	B8	SBU2
A6	Dp1	B7	Dn2
A7	Dn1	B6	Dp2
A8	SBU1	B5	CC2
A9	VBUS	B4	VBUS
A10	SSRXn2	B3	SSTXn2
A11	SSRXp2	B2	SSTXp2
A12	GND	B1	GND

Co-lay with U7305



14 BOP

緯創資通 Wistron Corporation

EXT IO (Thunderbolt(3)/Type C Conn)

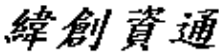
Doc: A34S/A3SS

SB

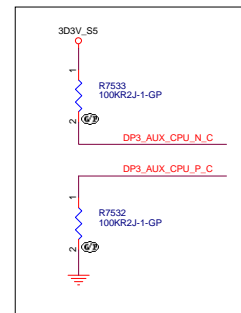
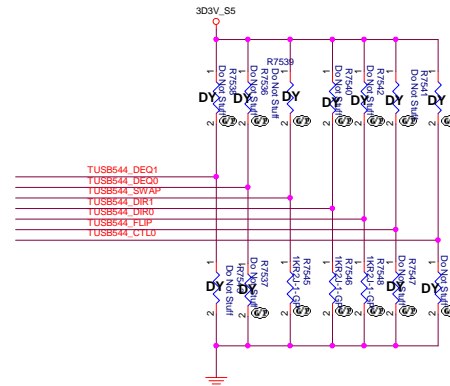
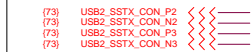


Main Func = TypeC

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From CPU



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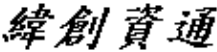
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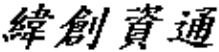
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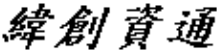
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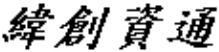
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Title <b>UNUSED PARTS (RSVD)</b>			
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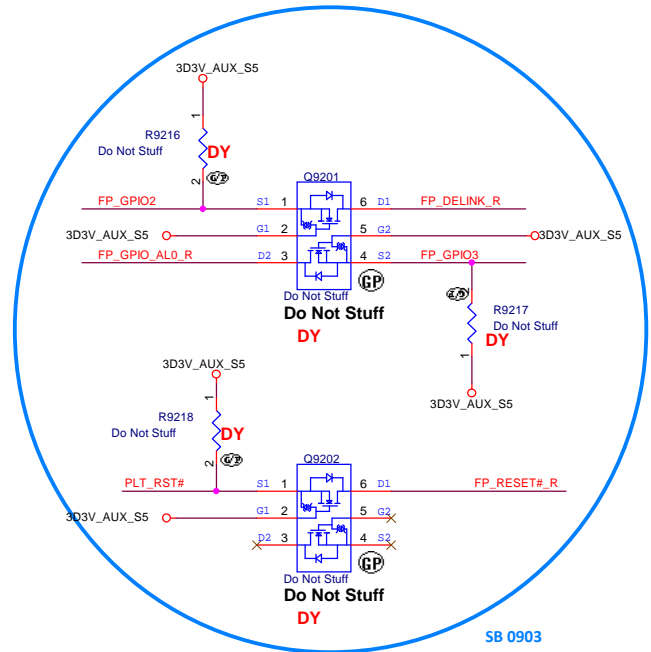
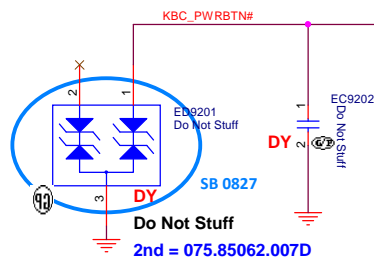
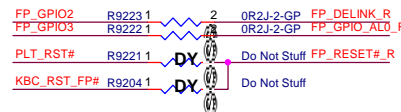
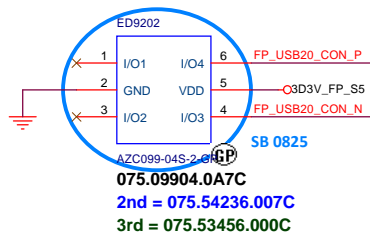
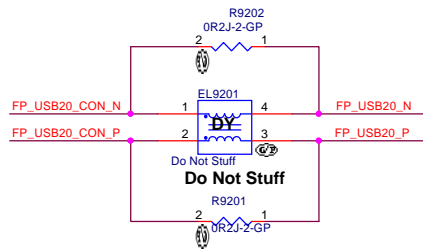
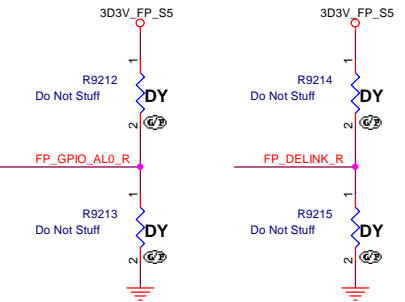
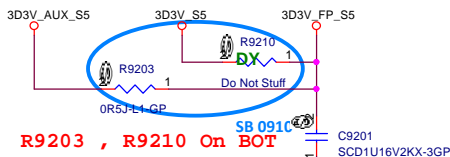
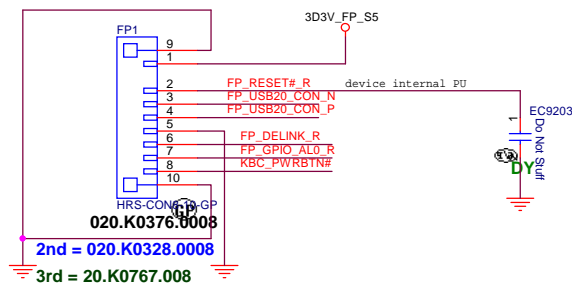
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# Main Func = Finger Printer

(18) FP\_USB20\_P <<<>>>=  
 (18) FP\_USB20\_N <<<>>>=  
 (24,65,89) KBC\_PWRBTN# >>>=  
 (24) FP\_GPIO2 >>>=  
 (24) FP\_GPIO3 >>>=  
 (58,72,89) PLT\_RST# >>>=  
 (24) KBC\_RST\_FP# >>>=





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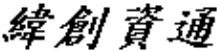
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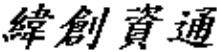
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Title <b>Commercial (RSVD)</b>			
Size A4	Document Number <b>A34S/A35S</b>		Rev <b>SB</b>
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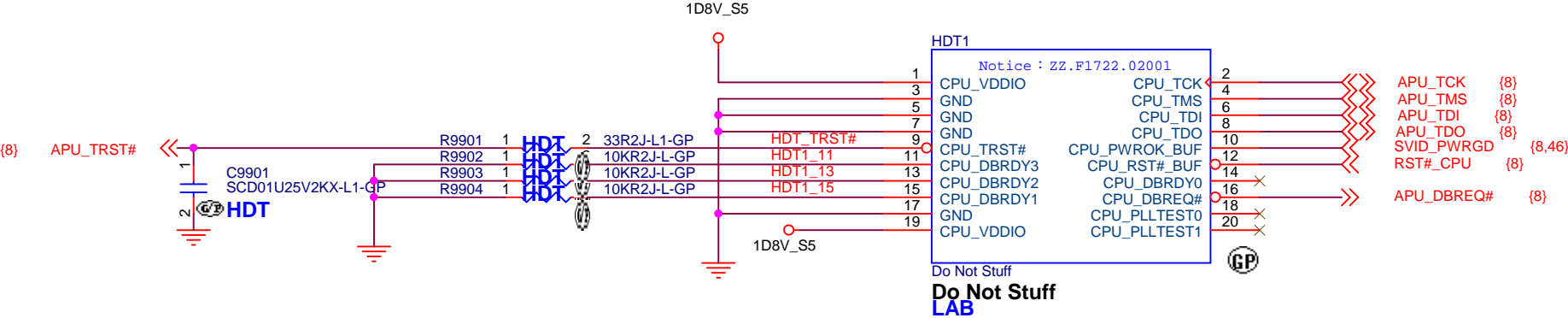
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HDT Connector



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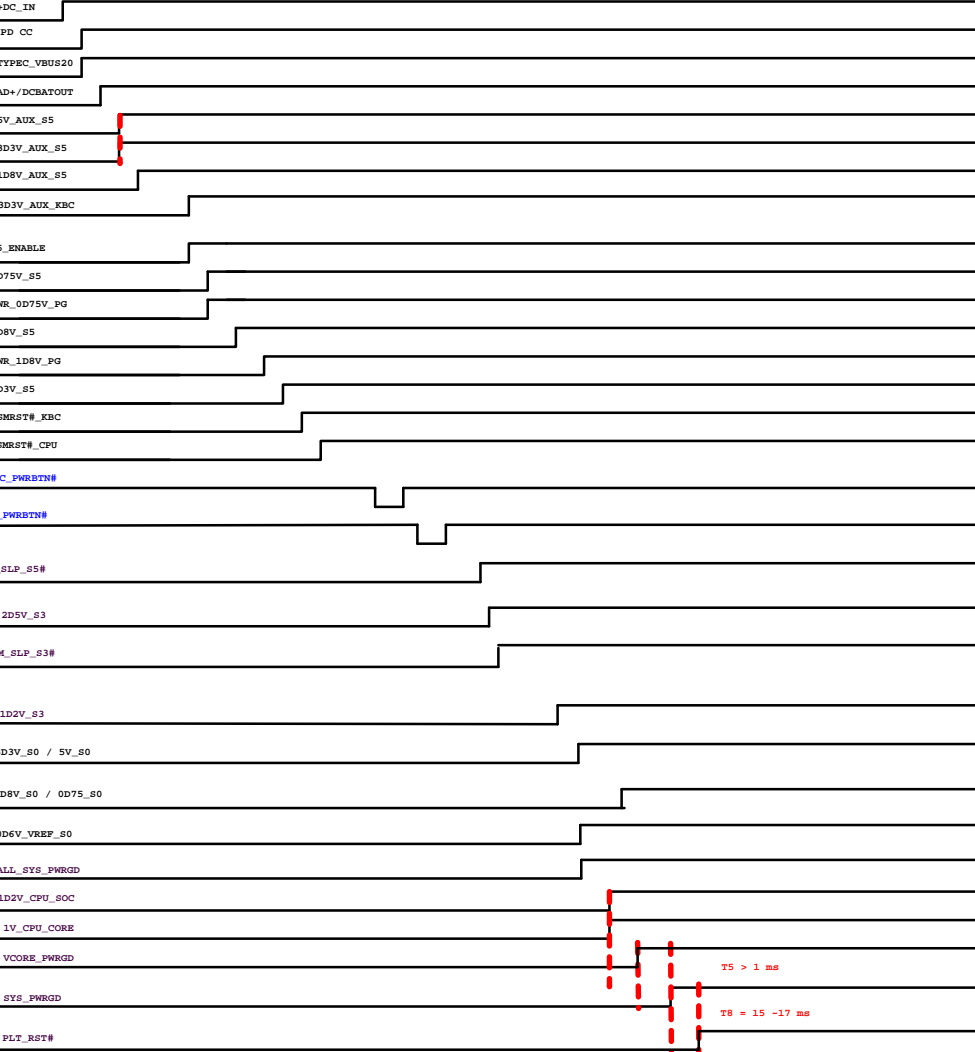
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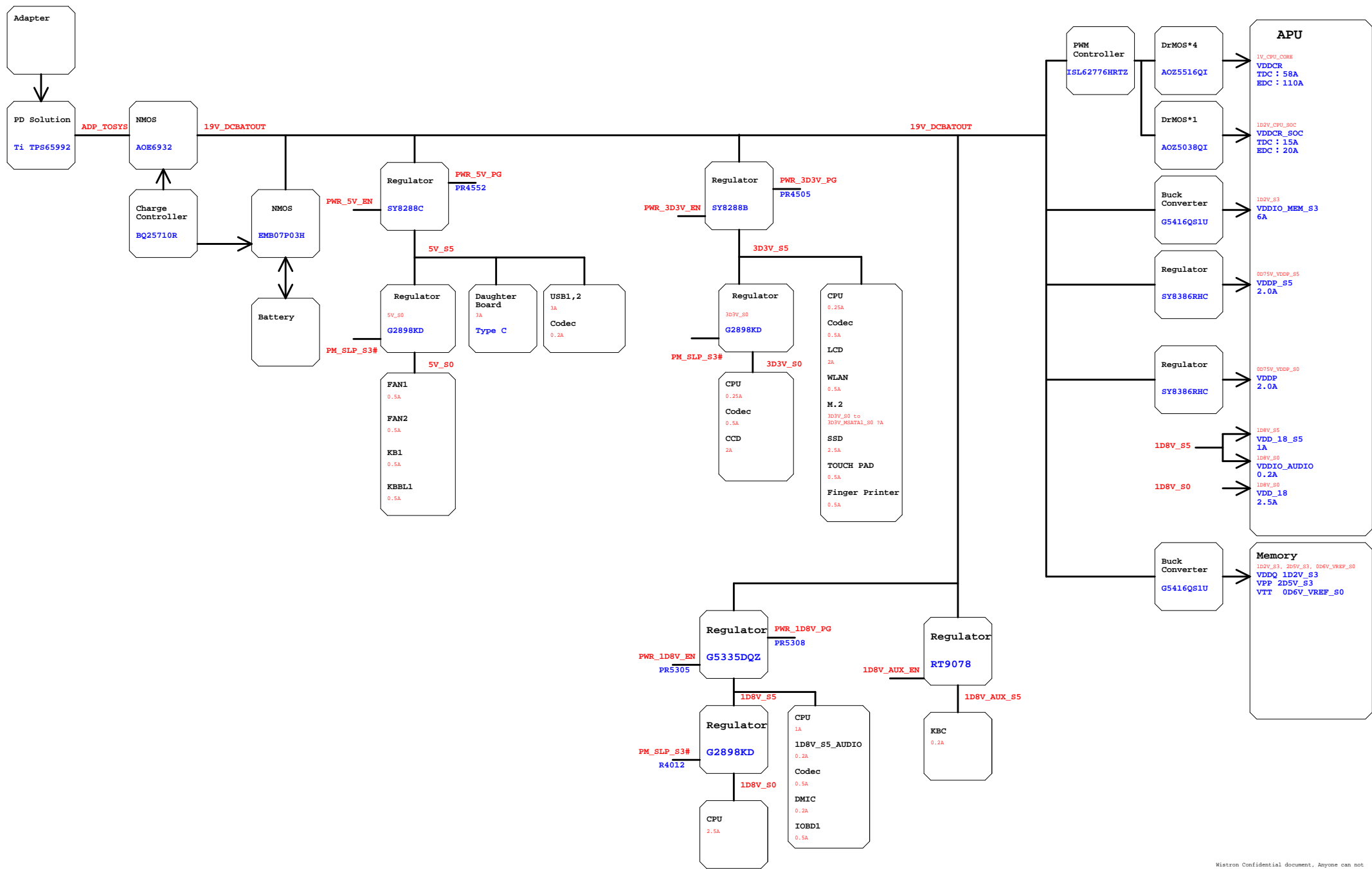
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AC mode

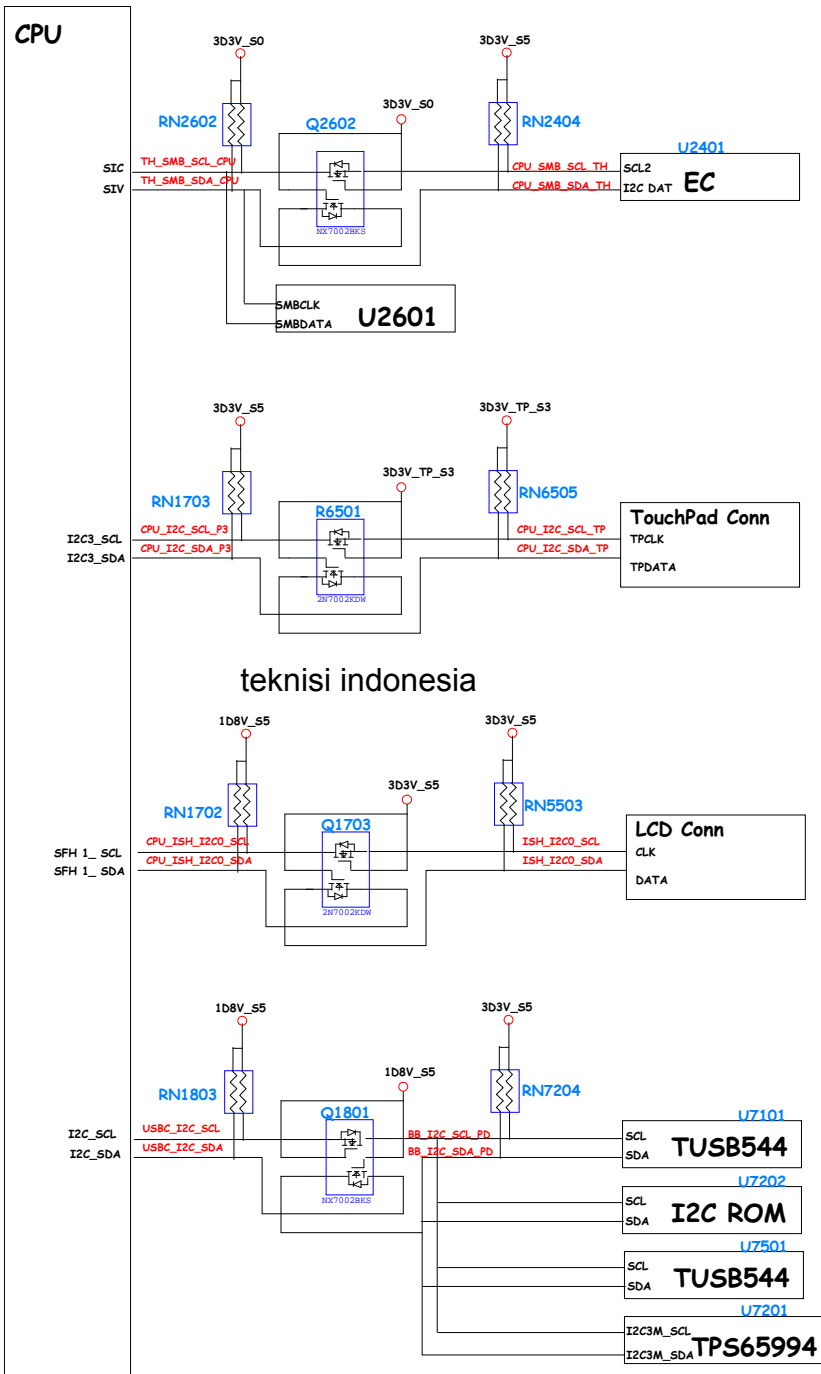
AD+ / DCBATOUT



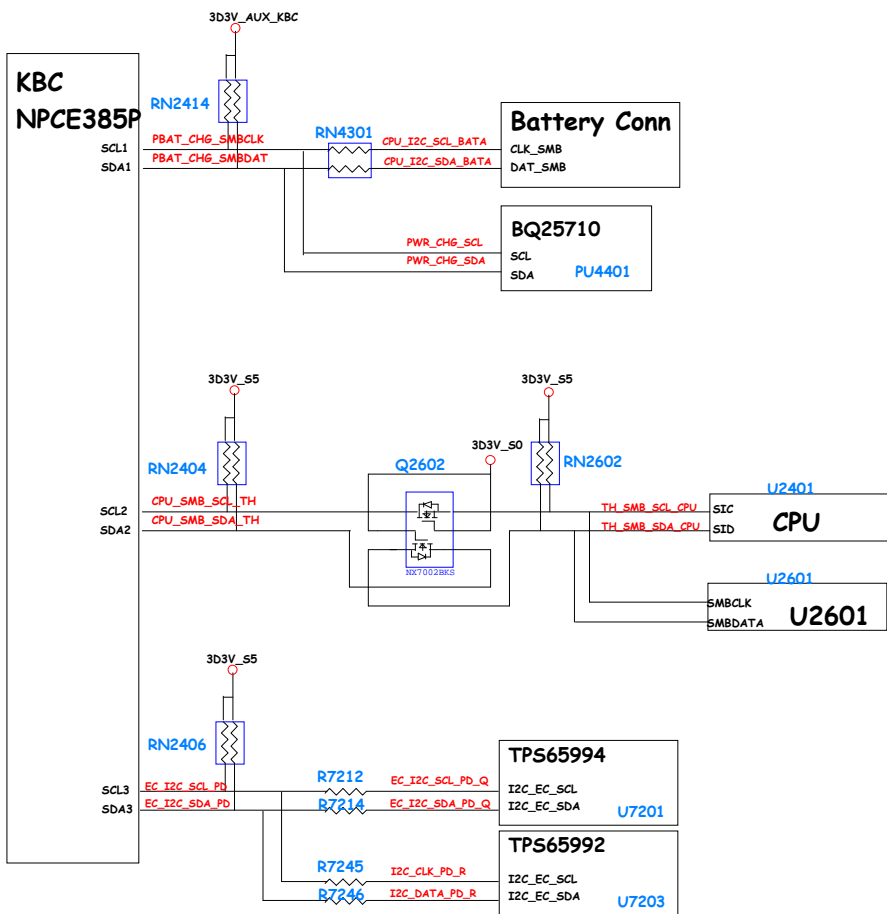
14 SDP



SMBus/I2C Block Diagram

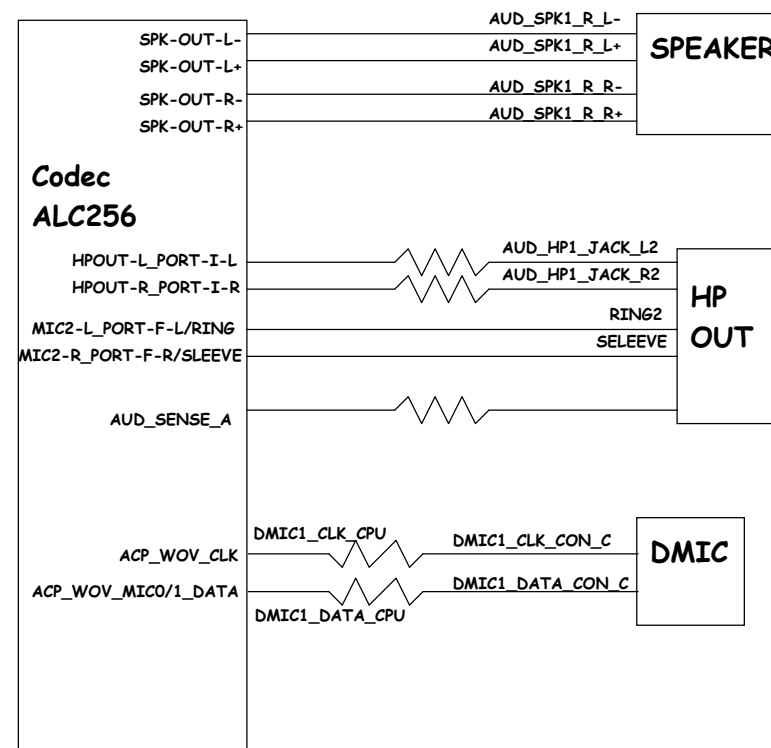


KBC SMBus/I2C Block Diagram

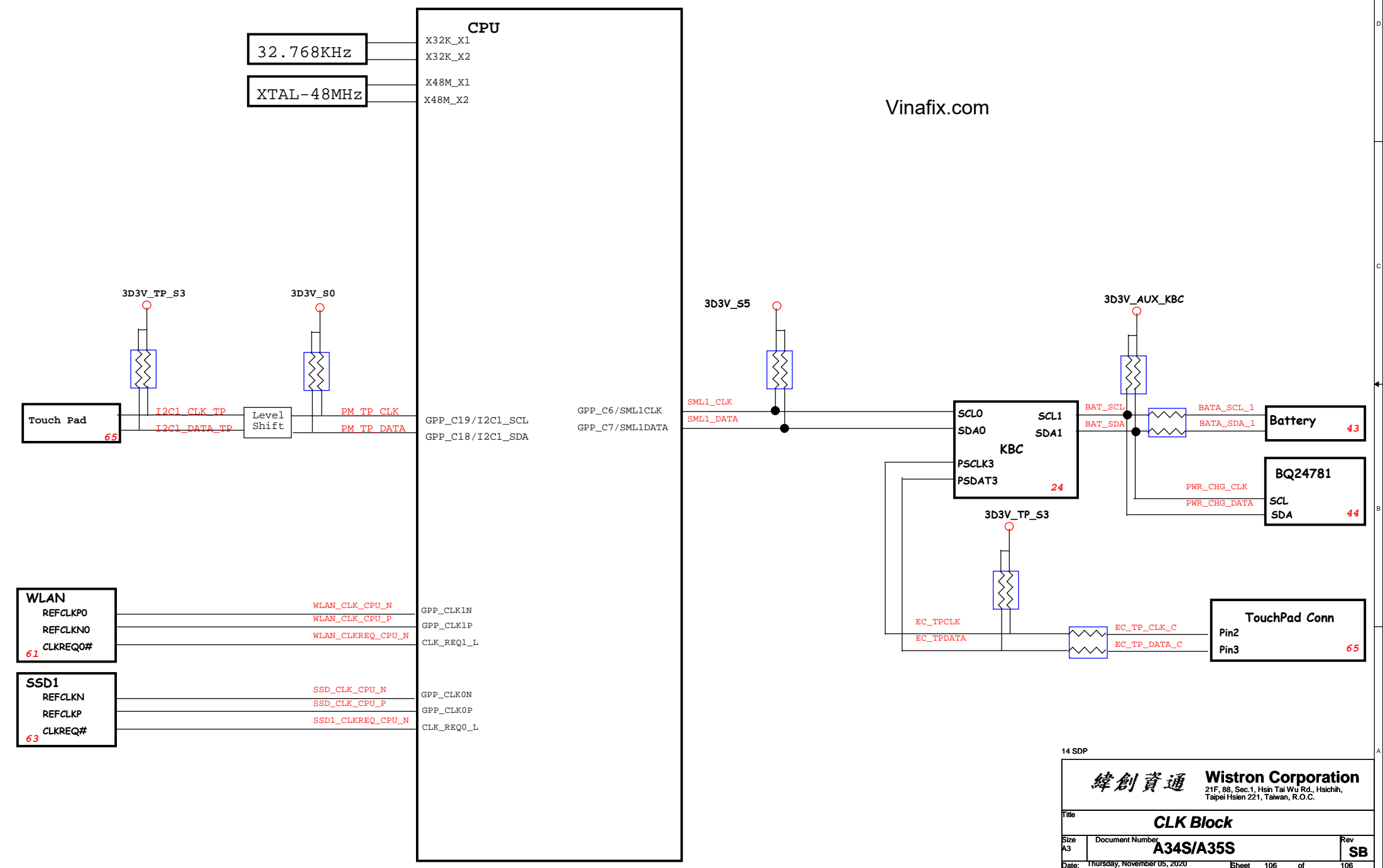


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## Audio Block Diagram



# CLOCK BLOCK DIAGRAM



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